

**ADS-631-153
Operating Instructions**

**4/25/00
Revision – B**

Meret Optical Communications, Inc.

**** WARNING ****

This synthesizer contains devices that are static-sensitive. Extreme caution must be exercised when handling this synthesizer or damage to the GaAs parts will result.



OPERATING INSTRUCTIONS

ADS-631-153 Ultra-Clean DDS Frequency Synthesizer

1. PRODUCT DESCRIPTION

The ADS-631-153 is a GaAs-based 500 MHz direct digital synthesizer (DDS) that operates from 1 MHz to 230 MHz with <0.12 Hz frequency resolution. A custom GaAs gate array is used to achieve the wide frequency bandwidth, fine resolution, and fast switching speed of the ADS-631-153. This configuration contains the three major devices that make up a direct digital synthesizer (Accumulator, ROM, and DAC) and a low pass filter on the output. The “-153” version refers to the addition of an external TTL-ECL converter board to allow control from a TTL interface.

2. PERFORMANCE/SPECIFICATIONS

Output Frequency

Range 1 MHz to 230 MHz
Resolution 0.1164... Hz ($500 \text{ MHz} \div 2^{32}$)
Control 31 parallel BINARY bits (pos-true TTL logic) w/ STROBE

Frequency Switching

Switching Speed <33.5 clock cycles plus filter delay (~3 nsec) = 70 nsec

Main Output (J1)

Level -4 dBm into 50Ω
Accuracy/Flatness ±3 dB

Monitor Output (J2)

Level -4 dBm into 50Ω
Accuracy/Flatness ±3 dB
Characteristics Unfiltered and compliment of main RF Out (180°)

Spectral Purity

Harmonics -35 dBc
Spurious -45 dBc (1-230 MHz), -60 dBc (F_{out} and $F_{\text{spur}} < 125 \text{ MHz}$)
Phase Noise (ext 500 MHz) per external clock

Reference Frequency

External (J4) 500 MHz @ +10 dBm ± 2 dB into 50Ω

Connectors — ADS-631

Main RF Output SMA Female (J2)
Monitor RF Output SMA Female (J3)
Ext DDS Clock Input SMA Female (J4)
Frequency Control 50-pin male subminiature D-connector (J1)

Power Supply (max)

ADS-631-103 -5.2V @ 4 A; +5V @ 250 mA; -12V @ 150 mA
TTL/ECL Converter (-153) +5V @ 90 mA; -5.2V @ @ 265 mA



2. PERFORMANCE/SPECIFICATIONS (continued)

Environmental

Operating Temp..... 0°C to +50°C

Storage Temp..... -20°C to +70°C

Dimensions 5"(W) x 7.08"(D) x 1.125"(H) = 4.5" x 6.5" PCB

Weight..... 1 lbs (0.9 kg), net; 3 lbs (1.4 kg), shipping

3. MECHANICAL CONFIGURATION

The ADS-631-153 is built according to best commercial practice. The top cover of the DDS module is used to help dissipate the heat generated by the synthesizer. SMA female connectors are used for interfacing with the RF signals and subminiature "D" connectors are used for interfacing with the frequency control and power supply lines. The TTL-ECL converter PCB is mounted to the top of the module and the ECL output of the converter PCB is connected to the ADS-631-103 module via a supplied 50-pin jumper cable.

IMPORTANT NOTE

The three GaAs devices that make up the synthesizer consume >15 watts of power. Heat sinking is employed to aid in heat dissipation but it is important that air be passed over the module in order to further reduce the heat build up.

4. INSTALLATION

The main output is obtained from the SMA connector on the DDS module, marked J2 and a monitor output is available at J3. Power is applied to the 4-pin header (JP1) on the PCB and the TTL controls are supplied to the 50-pin connector on the PCB. **Pin 1 on the power connector (JP1) is located farthest from the JP1 label.**

WARNING

Due to the static sensitivity of some of the synthesizer components, it is important that all the necessary precautions are taken to prevent static damage including but not limited to the use of ground straps and proper grounding techniques. Ground connections must be made first before connecting the frequency control mating connector to discharge any built-up static charge.

An external 500 MHz signal @ +10 dBm ± 2 dB is required for the correct operation



of the ADS-631.

5. POWER SUPPLY CONNECTIONS AND REQUIREMENTS

Three (3) DC power supplies must be supplied to the 4-pin IDC header on the TTL-ECL converter board.

Power Supply	Pin (JP1)	Current (Max)
-5.2V	4	4.3 A
-12V	2	150 mA
+5V	3	340 mA
GND	1	N/A

Table 4.1

The power for the ADS-631-103 module is derived from the PCB. The following pin assignments are shown for the connector (J1) on the module for reference only.

Power Supply	Pin (J1)	Current (Max)
-5.2V	17, 33, 50	4 A
-12V	32, 49	150 mA
+5V	44, 48	250 mA
GND	34, 39	N/A

Table 4.2

*** CAUTION ***

Some of the power supply lines are used without regulation so care must be taken not to connect an incorrect voltage to them. Supplying an incorrect polarity or incorrect voltage to these pins will result in destroying the internal circuitry and will void the warranty.

6. SIGNAL CONNECTIONS

The connectors on the DDS module are listed in the following table:

Signal	Level	Connector	
		Label	Type
Frequency/Phase Control	TTL	J1	50-pin submini "D"
Main RF Output	-4 dBm ± 3 dB	J2	female SMA
Monitor Output	-4 dBm ± 3 dB	J3	female SMA
DDS Clock Reference In	10dBm+2dB	J4	female SMA

Table 5.1



MAIN RF OUTPUT — The J2 connector is a filtered output from the 14-bit DAC providing approximately $-4 \text{ dBm} \pm 3 \text{ dB}$ output power up to 200 MHz. The LPF is set to approximately 230 MHz.

MONITOR OUTPUT — The J3 connector is an unfiltered complementary output from the DAC. This signal is 180° out of phase with the MAIN RF Output and provides approximately $-4 \text{ dBm} \pm 3 \text{ dB}$ output power. Note that alias components of the main output will be present in this output.

7. BINARY FREQUENCY CONTROL

A 32-bit, parallel, positive-true ECL logic level buss is normally used to control the ADS-631-153 DDS module. All logic is 10k ECL compatible with internal pull-down resistors to -2V . An optional TTL-ECL converter board has been provided as an external PCB mounted to the outside of the module therefore all control logic is TTL compatible.

Only synchronous programming control is available. Data must first be latched into a bank of internal registers before the output frequency can be updated with the STROBE (pin 18 for frequency and pin 47 for phase).

Pull any of the 32 bits for frequency (F00 through F31) and/or any of the 4 bits for phase (P0 through P3) to a high TTL level for the frequency (and/or phase) desired. All other bits should be pulled to a low TTL level. Refer to table 5.1 for a description of all of the pin assignments. Note that F31 should normally be grounded as it controls the Nyquist frequency ($f_{\text{clk}} \div 2$).

Pulse the LATCH line (pin 2) and data will be loaded into the internal registers on the rising edge of the LATCH pulse. Data is then ready to be strobed into the phase accumulator one clock cycle after the rising edge of the **FREQ STROBE** pulse. The setup and hold times for the LATCH and data is 12 nsec. If desired, the LATCH can be tied HIGH so only the **FREQ STROBE** is needed.

The output frequency will change 33.5 clock cycles after the rising edge of the frequency **STROBE** pulse plus any delay due to the low pass filter (under 3 nsec for a 220 MHz low pass filter.) The output phase will be updated 17.5 clock cycles after the rising edge of the phase **STROBE** (pin 47).



8. PHASE CONTROL

Four bits of phase control are available on the ADS-632-153. This represents a 22.5° resolution and programming is accomplished in a similar manner as the frequency control except that the PHASE STROBE (Pin 47) is used to load data into the unit. (Note that the LATCH line is not used for phase control). Setup and Hold times for the data is 12 nsec. There is a 17.5 clock delay from the PHASE STROBE to the output.

9. RESET

In addition to the frequency control, a separate TTL control line is provided to allow for very fast control of output level. When activated by pulling the control line to a TTL HIGH, the output signal will be attenuated by over 100 dB. Since all inputs are pulled down to ground, it is not necessary to pull the RESET to a low TTL level to turn on the output.

RESET is used when it is desirable to have the phase accumulator continue even though no output is present. When RESET is released to turn the output signal on, the phase of the signal will be identical to the phase of the output as if the output had not been turned off (Phase coherence has been maintained). The output will be turned off 2.5 clock cycles (plus the LPF delay) after rising edge.

Since the resolution of the synthesizer is "limited" to a non standard step size, some frequency values may not be available. Any frequency, however, will be settable to an accuracy of less than the smallest step size ($500\text{MHz} \div 2^{32}$).



10. PROGRAMMING CONTROL LINES FOR THE TWO MODULES

FREQUENCY CONTROL (J1)			PHASE CONTROL (J1)	
<u>Frequency</u>	<u>Bit#</u>	<u>Pin#</u>	<u>Phase</u>	<u>Pin #</u>
$f_{clk} \div 2^1$	F31	30	180°	14
$f_{clk} \div 2^2$	F30	13	90°	31
$f_{clk} \div 2^3$	F29	46	45°	15
$f_{clk} \div 2^4$	F28	29	22.5°	16
$f_{clk} \div 2^5$	F27	12		
$f_{clk} \div 2^6$	F26	45		
$f_{clk} \div 2^7$	F25	28		
$f_{clk} \div 2^8$	F24	11		
$f_{clk} \div 2^9$	F23	27		
$f_{clk} \div 2^{10}$	F22	10		
$f_{clk} \div 2^{11}$	F21	43		
$f_{clk} \div 2^{12}$	F20	26		
$f_{clk} \div 2^{13}$	F19	9		
$f_{clk} \div 2^{14}$	F18	42		
$f_{clk} \div 2^{15}$	F17	25		
$f_{clk} \div 2^{16}$	F16	8		
$f_{clk} \div 2^{17}$	F15	41		
$f_{clk} \div 2^{18}$	F14	24		
$f_{clk} \div 2^{19}$	F13	7		
$f_{clk} \div 2^{20}$	F12	40		
$f_{clk} \div 2^{21}$	F11	23		
$f_{clk} \div 2^{22}$	F10	6		
$f_{clk} \div 2^{23}$	F09	22		
$f_{clk} \div 2^{24}$	F08	5		
$f_{clk} \div 2^{25}$	F07	38		
$f_{clk} \div 2^{26}$	F06	21		
$f_{clk} \div 2^{27}$	F05	4		
$f_{clk} \div 2^{28}$	F04	37		
$f_{clk} \div 2^{29}$	F03	20		
$f_{clk} \div 2^{30}$	F02	3		
$f_{clk} \div 2^{31}$	F01	36		
$f_{clk} \div 2^{32}$	F00	19		

POWER (J1) - REF ONLY	
<u>DC Voltage</u>	<u>Pin#</u>
-5.2V	17,33,50
-12V	32,49
+5V	44,48

POWER (JP1)	
<u>DC Voltage</u>	<u>Pin#</u>
-5.2V	4
-12V	2
+5V	3
GND	1

OTHER DDS MODULE PINS (J1)	
FREQ STROBE	18
PHASE STROBE	47
RESET	35
LATCH	2
GROUND	34, 39
No Connect	6



ADS-631-153 OPERATING INSTRUCTIONS

11. WARRANTY

All Meret products are warranted against defects in material and workmanship for a period of one year after initial shipment. Meret will repair or replace any circuit or component that is found to be defective during this period if in Meret's sole opinion the product is deemed defective.

Any modifications or options performed by Meret during the initial one-year period shall be included under the initial warranty, and such secondary warranties shall terminate one year after the initial shipment. Shipment of the product to Meret (San Diego, CA) shall be made prepaid and shall not be made without prior authorization by Meret.

This warranty is voided if the product is abused or if the user makes unauthorized modifications.

This warranty is in lieu of all other warranties, expressed or implied, and no person is authorized to represent or assume for Meret any liability in connection with the sales of our products other than stated within this warranty.

Serial Number

Options: _____

Remarks: _____

QC by _____ Date: _____

