

**ADS-632-153  
Operating Instructions**

**10/31/00  
Revision B D**

**Meret Optical Communications, Inc.**

**\*\* WARNING \*\***

*This synthesizer contains devices that are static-sensitive. Extreme caution must be exercised when handling this synthesizer or damage to the GaAs parts will result.*





**2. PERFORMANCE/SPECIFICATIONS (continued)**

**Frequency Switching**

Switching Speed ..... <33.5 clock cycles plus filter delay (~3 nsec) = 70 nsec

**Connectors — ADS-631**

Main RF Output ..... SMA Female (J2)  
 Monitor RF Output ..... SMA Female (J3)  
 Ext DDS Clock Input..... SMA Female (J4)  
 Frequency Control ..... 50-pin male subminiature D-connector (J1)

**Connectors — 500 MHz Clock Reference**

Ext 10 MHz REF Input..... SMA Female (J1)  
 Ext 10 MHz REF Output..... SMA Female (J2)  
 Auxiliary DDS Clock Output.. SMA Female (J3)  
 DDS Clock Output..... SMA Female (J5)  
 Spare ..... SMA Female (J4)  
 Power ..... 9-pin subminiature male D-connector (P1)

**Environmental**

Operating Temp ..... 0°C to +50°C  
 Storage Temp..... -20°C to +70°C

**Power Supply (max)**

ADS-631-153..... -5.2V @ 4 A; +5V @ 250 mA; -12V @ 150 mA;  
 500 MHz Reference Gen ..... +5V @ 350 mA; +12V @ 100 mA  
 TTL/ECL Converter ..... +5V @ 90 mA; -5.2V @ @ 265 mA

**Dimensions** ..... 5"(W) x 7.08"(D) x 2.25"(H) plus TTL/ECL PCB

**Weight**..... 2 lbs (0.9 kg), net; 3 lbs (1.4 kg), shipping

**3. MECHANICAL CONFIGURATION**

The ADS-632-153 is built according to best commercial practice. The two modules mounted on a plate that form the product are the DDS module and the Clock reference (500MHz) module. The top cover of the DDS module is used to help dissipate the heat generated by the synthesizer. SMA female connectors are used for interfacing with the RF signals and subminiature “D” connectors are used for interfacing with the frequency control and power supply lines. The 4.5” x 6.5” PCB to convert TTL control supplied by the user to the necessary ECL logic required by the synthesizer is mounted to the cover of the reference generator.

**IMPORTANT NOTE**

The three GaAs devices that make up the synthesizer consume >15 watts of power. Heat sinking is employed to aid in heat dissipation but it is important that air be passed over the module in order to further reduce the heat build up.



#### 4. INSTALLATION

The main output is obtained from the SMA connector on the DDS module, marked J2 and a monitor output is available at J3.

**\*WARNING\***

Due to the static sensitivity of some of the synthesizer components, it is important that all the necessary precautions are taken to prevent static damage including but not limited to the use of ground straps and proper grounding techniques. Ground connections must be made first before connecting the frequency control mating connector to discharge any built-up static charge.

The ADS-632 is supplied with an internal 10 MHz ( $\pm 1$  ppm) TCXO. If an external 10 MHz reference is supplied, it must be connected to J1 on the Reference Module with 0 dBm  $\pm$  2 dB level. A 10 MHz output is provided but it is not buffered so connecting this output (J2) to 50 $\Omega$  can result in the unit unlocking. The unit will then have the stability of the internal free-running crystal (~100 ppm). If the internal 10 MHz is desired, **remove** any signal from J1 of the reference module and short pins 2 & 4 of the 9-pin connector together on the 500 MHz Reference Generator module to supply +12V to the +5V voltage regulator for the internal crystal. If desired, this power can be internally hardwired, so that if no external reference will ever be used, the external wiring would be unnecessary.

The 10 MHz output is supplied at a  $>-15$  dBm level.

#### 5. POWER SUPPLY CONNECTIONS AND REQUIREMENTS

Three (3) DC power supplies must be supplied to the 4-pin IDC header on the TTL-ECL converter board.

Power Supply	Pin (JP1)	Current (Max)
-5.2V	4	4.3 A
-12V	2	150 mA
+5V	3	340 mA
GND	1	N/A

Table 4.1

**Pin 1 on the power connector (JP1) is located farthest from the JP1 label.**



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The 50-pin flat-ribbon cable supplies the necessary voltages to the DDS module on the following pins (do not supply voltage to these pins):

Power Supply	Pin (J1)	Current (Max)
-5.2V	17, 33, 50	4 A
-12V	32, 49	150 mA
+5V	44, 48	250 mA
GND	34, 39	N/A

Table 4.2

Two DC power supplies must be supplied to the 9-pin subminiature "D" connector on the **clock reference module**. They are defined as follows:

Power Supply	Pin (P1)	Current (Max)
+5V	1	350 mA
+12V	9	100 mA
GND	7,8	N/A

Table 4.2

### \* CAUTION \*

Some of the power supply lines are used without regulation so care must be taken not to connect an incorrect voltage to them. Supplying an incorrect polarity or incorrect voltage to these pins will result in destroying the internal circuitry and will **void the warranty**.

## 6. SIGNAL CONNECTIONS

The connectors on the DDS module are listed in the following table:

Signal	Level	Connector	
		Label	Type
Frequency/Phase Control	N/A	J1	50-pin submini "D"
Main RF Output	-4 dBm $\pm$ 3 dB	J2	female SMA
Monitor Output	-4 dBm $\pm$ 3 dB	J3	female SMA
DDS Clock Reference In	>+5 dBm	J4	female SMA

Table 5.1



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**MAIN RF OUTPUT** — The J2 connector is a filtered output from the 14-bit DAC providing approximately  $-4 \text{ dBm} \pm 3 \text{ dB}$  output power up to 200 MHz. The LPF is set to approximately 230 MHz.

**MONITOR OUTPUT** — The J3 connector is an unfiltered complementary output from the DAC. This signal is  $180^\circ$  out of phase with the MAIN RF Output and provides approximately  $-4 \text{ dBm} \pm 3 \text{ dB}$  output power. Note that alias components of the main output will be present in this output.

The connectors on the Clock Reference module are listed in the following table:

Signal	Level	Connector	
		Label	Type
Power Supply	N/A	P1	9-pin submini "D"
10 MHz Input	$0 \text{ dBm} \pm 2 \text{ dB}$	J1	female SMA
10 MHz Output	$>-15 \text{ dBm}$	J2	female SMA
500 MHz Output	$>+10 \text{ dBm}$	J3	female SMA
Not Used	N/A	J4	female SMA
500 MHz Output	$+5 \text{ dBm}$	J5	female SMA

Table 5.2

### 7. BINARY FREQUENCY CONTROL

A 32-bit, parallel, positive-true ECL logic level buss is used to control the ADS-632-103 DDS module. All logic is 10k ECL compatible with internal pull-down resistors to  $-2\text{V}$ . Note that an optional TTL-ECL converter board is available as an external PCB mounted to the outside of the module. Please consult the factory for additional details. A TTL-ECL converter board is included in the -153 option. The user supplies TTL level logic.

Only synchronous programming control is available. Data must first be latched into a bank of internal registers before the output frequency can be updated with the STROBE (pin 18 for frequency and pin 47 for phase).

Pull any of the 32 bits for frequency (F00 through F31) and/or any of the 4 bits for phase (P0 through P3) to a high TTL level for the frequency (and/or phase) desired. All other bits should be pulled to a low TTL level. Refer to table 5.1 for a description of all of the pin assignments. Note that F31 should normally be grounded as it controls the Nyquist frequency.



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Since the resolution of the synthesizer is "limited" to a non standard step size, some frequency values may not be available. Any frequency, however, will be settable to an accuracy of less than the smallest step size ( $500\text{MHz} \div 2^{32}$ ).

Pulse the LATCH line (pin 2) and data will be loaded into the internal registers on the rising edge of the LATCH pulse. Data is then ready to be strobed into the phase accumulator one clock cycle after the rising edge of the FREQ STROBE pulse. The setup and hold times for the LATCH and data is 2 nsec. If desired, the LATCH can be tied HIGH so only the FREQ STROBE is needed.

The output frequency will change 33.5 clock cycles after the rising edge of the frequency STROBE pulse plus any delay due to the low pass filter (under 3 nsec for a 220 MHz low pass filter.) The output phase will be updated 17.5 clock cycles after the rising edge of the phase STROBE (pin 47). DATA and LATCH signal require a Setup and hold time of 12 nsec.

### 8. PHASE CONTROL

Four bits of phase control are available on the ADS-632-153. This represents a  $22.5^\circ$  resolution and programming is accomplished in a similar manner as the frequency control except that the PHASE STROBE (Pin 47) is used to load data into the unit. (Note that the LATCH line is not used for phase control). Setup and Hold times for the data is 12 nsec. There is a 17.5 clock delay from the PHASE STROBE to the output.

### 9. RESET

In addition to the frequency control, an ECL control line is provided to allow for very fast control of output level. When activated by pulling the control line to an ECL HIGH, the output signal will be attenuated by over 100 dB. Since the input is pulled down to -2V, it is not necessary to pull the RESET to a low ECL level to turn on the output.

RESET is used when it is desirable to have the phase accumulator continue even though no output is present. When RESET is released to turn the output signal on, the phase of the signal will be identical to the phase of the output as if the output had not been turned off (Phase coherence has been maintained). The output will be turned off 2.5 clock cycles (plus the LPF delay) after rising edge.



10. PROGRAMMING CONTROL LINES FOR THE TWO MODULES

FREQUENCY CONTROL (J1)			PHASE CONTROL (J1)	
<u>Frequency</u>	<u>Bit#</u>	<u>Pin#</u>	<u>Phase</u>	<u>Pin #</u>
$f_{clk} \div 2^1$	F31	30	180°	14
$f_{clk} \div 2^2$	F30	13	90°	31
$f_{clk} \div 2^3$	F29	46	45°	15
$f_{clk} \div 2^4$	F28	29	22.5°	16
$f_{clk} \div 2^5$	F27	12		
$f_{clk} \div 2^6$	F26	45		
$f_{clk} \div 2^7$	F25	28		
$f_{clk} \div 2^8$	F24	11		
$f_{clk} \div 2^9$	F23	27		
$f_{clk} \div 2^{10}$	F22	10		
$f_{clk} \div 2^{11}$	F21	43		
$f_{clk} \div 2^{12}$	F20	26		
$f_{clk} \div 2^{13}$	F19	9		
$f_{clk} \div 2^{14}$	F18	42		
$f_{clk} \div 2^{15}$	F17	25		
$f_{clk} \div 2^{16}$	F16	8		
$f_{clk} \div 2^{17}$	F15	41		
$f_{clk} \div 2^{18}$	F14	24		
$f_{clk} \div 2^{19}$	F13	7		
$f_{clk} \div 2^{20}$	F12	40		
$f_{clk} \div 2^{21}$	F11	23		
$f_{clk} \div 2^{22}$	F10	6		
$f_{clk} \div 2^{23}$	F09	22		
$f_{clk} \div 2^{24}$	F08	5		
$f_{clk} \div 2^{25}$	F07	38		
$f_{clk} \div 2^{26}$	F06	21		
$f_{clk} \div 2^{27}$	F05	4		
$f_{clk} \div 2^{28}$	F04	37		
$f_{clk} \div 2^{29}$	F03	20		
$f_{clk} \div 2^{30}$	F02	3		
$f_{clk} \div 2^{31}$	F01	36		
$f_{clk} \div 2^{32}$	F00	19		

  

DDS/Converter POWER (JP1)	
<u>DC Voltage</u>	<u>Pin#</u>
-5.2V	4
-12V	2
+5V	3
GND	1

  

500 MHz POWER (P1)	
<u>DC Voltage</u>	<u>Pin#</u>
+5V	1
+12V	9
GROUND	7, 8

  

OTHER DDS MODULE PINS (J1)	
FREQ STROBE	18
PHASE STROBE	47
RESET (unused)	1*
RESET	35
LATCH	2
GROUND	34, 39

  

OTHER REF MODULE PINS (P1)	
+12V IN for Ref	4
+12V OUT for Ref	2
No Connect	5
No Connect	3, 6

\* This control line is shown since previous operating instructions included this line. This reset line is now internally grounded and should not be controlled.



ADS-632-153 OPERATING INSTRUCTIONS

11. WARRANTY

All Meret products are warranted against defects in material and workmanship for a period of one year after initial shipment. Meret will repair or replace any circuit or component that is found to be defective during this period if in Meret's sole opinion the product is deemed defective.

Any modifications or options performed by Meret during the initial one-year period shall be included under the initial warranty, and such secondary warranties shall terminate one year after the initial shipment. Shipment of the product to Meret (San Diego, CA) shall be made prepaid and shall not be made without prior authorization by Meret.

This warranty is voided if the product is abused or if the user makes unauthorized modifications.

This warranty is in lieu of all other warranties, expressed or implied, and no person is authorized to represent or assume for Meret any liability in connection with the sales of our products other than stated within this warranty.

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\_\_\_\_\_  
Serial Number

Options: \_\_\_\_\_

Remarks: \_\_\_\_\_

\_\_\_\_\_

QC by \_\_\_\_\_ Date: \_\_\_\_\_

