

OPERATING INSTRUCTIONS

SEI-1618EB-00 Technology Evaluation Kit

SEI-1618EB-01 Technology Evaluation Kit

1. PRODUCT DESCRIPTION

The SEI-1618EB evaluation card was designed to demonstrate Meret's ALL™ (fractional) technology. The ALL™ is a Meret patented fractional PLL circuit, and is fully programmable — i.e., both the counters AND THE FRACTIONALITY.

This single phase lock loop will produce phase noise performance at 1 kHz offsets and less of 20 dB better than can be predicted for other more traditional designs.

The ALL™ Technology Evaluation Kit consists of the 2.5" x 3.5" evaluation board, a 3.5" PC compatible floppy disk (Please call the factory if a 5.25" floppy is needed), a 6 foot printer extension cable, and this set of operating instructions. For more information on the ALL™ architecture, consult the factory for a listing of the published articles on this subject.

The SEI-1618EB-00 is a frequency synthesizer designed to operate at 1,750 MHz \pm 150 MHz with an external 10 MHz reference. The SEI-1618EB-01 is identical to the SEI-1618EB-00 except that it provides an internal \pm 2.5 ppm/year 10 MHz TCXO. This unit is based on our SEI-1618PG device that combines a traditional PLL with our unique patented Arithmetic Lock Loop (ALL™) design. The PLL section covers the overall operating range of the unit in 1.25 MHz steps for the SEI-1618EB-00 and the ALL™ circuit adds the remaining 250 kHz resolution. Due to the frequency range, the use of the ALL circuitry improves the phase noise performance by 10 dB over a traditional single loop design. Note that the fractionality (and therefore step size) is fully programmable but this evaluation board has been optimized for 250 kHz steps.

2. PERFORMANCE/SPECIFICATIONS (Typical)

Frequency

Range 1,600 MHz to 1,900 MHz

Step Size 250 kHz

Control 29-bit serial interface through provided software

Main Output

Level +7 dBm into 50 Ω

Flatness \pm 2 dB



SEI-1618EB-00 OPERATING INSTRUCTIONS

2. PERFORMANCE/SPECIFICATIONS (continued) -Typical

Spectral Purity

Harmonics.....<-20 dBc, typical
 Spurious.....<-60 dBc
 Phase Noise
 1 kHz offset<-80 dBc/Hz
 10 kHz offset<-80 dBc/Hz

Frequency Ref

SEI-1618EB-00..... 10 MHz, External @ +8 dBm ± 2 dB
 SEI-1618EB-01..... 10 MHz, Internal @ ±2.5 ppm/year

Lock Indicator “1” for Out-of-Lock (TTL compatible)

Connectors

RF Output (J2).....SMA female
 Ref Input (J1).....SMA female
 Freq Control (JP2)25-pin female subminiature “D”
 Power Supply (JP1)4-pin IDC header

Power Supply+5V @ 300 mA; +15V @ 150 mA

Environmental

Operating Temp.....0°C to +50°C
 Storage Temp.....-20°C to +70°C
 Dimensions2.5" x 3.5" x 0.4" printed circuit board
 Weight<1 lbs, net; 4 lbs, shipping

3. MECHANICAL CONFIGURATION

The SEI-1618EB is manufactured on a single printed circuit board with a 25-pin (male) subminiature “D” connector located on one 2.5” edge. Both the Ext Ref Input (SEI-1618EB-00 only) and the RF output are located on the other 2.5” edge of the board and a separate 4-pin IDC connector for the power supplies and lock detector is located near the 25-pin connector.

Function	Connector	Mating Connector
Serial Frequency Control	25-pin Submini “D”	Amphenol 117DB-25S or equivalent
RF Out	SMA female	SMA male
Ext Ref In*	SMA female	SMA male
Power Supply / LD	4-pin IDC header	4-pin IDC single row

* SEI-1618EB-00 only



4. POWER SUPPLY CONNECTIONS

Power is supplied to the following pins on the 4-pin IDC header (JP1):

Power Supply	Designation	Pin Numbers
+5V	V _{CC}	4
+15V	V _C	2
Ground	GND	1
Lock Detector	LD	3

Note that pin#1 is designated on the board with the square pad (on the solder side of the board.) It is also the pin closest to the 25-pin connector.

5. REFERENCE FREQUENCY

The SEI-1618EB-00 board has been designed to operate from an external 10 MHz reference at a level of +8 dBm ± 2 dB. If an internal 10 MHz reference with a stability and accuracy of ±2.5 ppm is desired, order the SEI-1618EB-01.

6. OPERATION

Although the synthesizer is specified over the 300 MHz range, the software supplied with the unit has no such limitation. Care should be taken to program frequencies within the 1,600-1,900 MHz range. Although the unit will operate outside this range, it has not been tested and there is no guarantee of performance.

The software supplied with the unit has been developed to simplify the evaluation process. However, the instructions that follow this section shall give adequate details should someone desire to also control the synthesizer directly through the serial port.

6.1 DEMONSTRATING THE SEI-1618EB

This section deals with operating the SEI-1618EB with the supplied software for control.

6.1.1 Hardware Setup

Connect the power supplies (+5V, +15V & GND) per section 4 above. If the SEI-1618EB-00 has been ordered, an external 10 MHz reference must be supplied to the SMA as shown on the following picture and the drawing on Page 13.

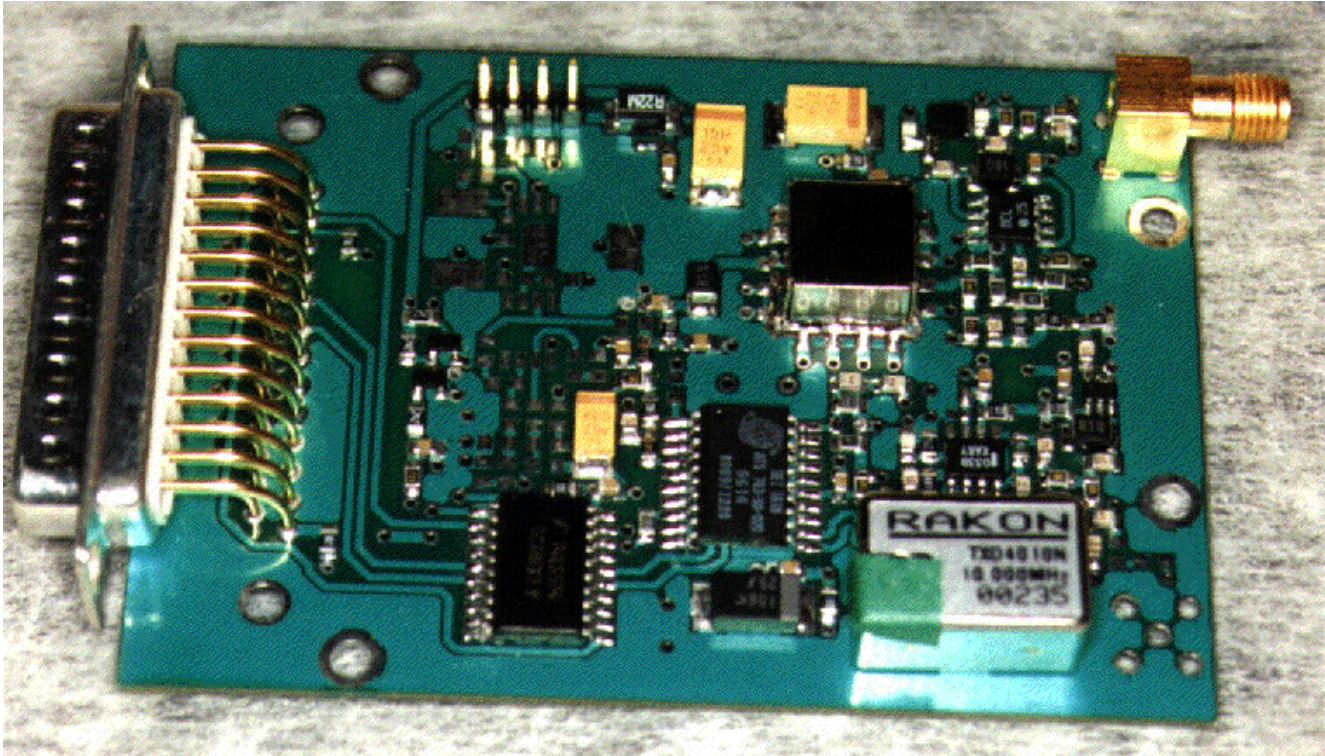


SEI-1618EB-00 OPERATING INSTRUCTIONS

25-Pin connector

Pin 1

RF Output



Ref IN (not shown) ↑

SEI-1618EB-01 Evaluation

Using the supplied printer extension cable (25-pin subminiature “D” male connector on one side and a 25-pin subminiature “D” female connector on the other side), connect the 25-pin connector on the evaluation board to the parallel printer port on the computer. If this cable is not available, it should be possible to connect the SEI-1618EB evaluation board directly to the printer output port on the computer.

6.1.2 Software Setup

Install the software in an IBM PC® AT or compatible or faster computer. There are no special system requirements for the demonstration software except that it will not operate properly from an IBM PC® or compatible computer (requires an 80286-based computer at least). The software may be run from the floppy disk directly or the file (1618.EXE) may be copied to your hard disk. Note that the software is a DOS based program.



SEI-1618EB-00 OPERATING INSTRUCTIONS

Use the following command syntax to copy the file to your hard disk and insert the correct disk letters as required. This statement assumes that the floppy disk is the “A” drive and the hard disk is the “C” drive. The “directory” is the subdirectory on the hard disk that will receive the program. If the directory does not already exist, you must create it first.

COPY A:1618.EXE C:\directory

Type the following command to start the program:

1618 <RETURN>

The Main control window for the Meret SEI-1618 will be displayed on the screen. It has been designed to set the default parameters for the SEI-1618EB-00 and allow the user to program the desired frequency.

Frequency (MHz)		
Desired Freq	[50]]
	K	[23]
	M	[13]
	N	[1]

Actual Freq: 49.9305555555

Re-Compute

Set Freq

Reference (MHz)		
Ref Freq	[10]]
	R	[6]
	F	[24]
	P	[16]

Defaults

Set Ref



6.1.3 Reference Selection

First the reference frequency into the phase detector, the fractionality and the size of the dual modulus must be programmed into the device. Normally this is needed only once and it must be done before any desired frequency is programmed.

Ref Freq	This represents the actual frequency used by the board. The default condition is 10 MHz which is the frequency supplied by the internal TCXO (SEI-1618EB-01) and is the correct frequency for the evaluation board.
R Register	This register is the programmable number that selects the actual frequency used by the phase detector. For the evaluation board, this number should be set to 8 for 1.25 MHz.
F Register	Note that if the demo software is not used, the actual number programmed into the register is one less than the desired number. This register selects the fractionality used by the SEI-1618. For the evaluation board, use 5 but note that this number can be selected from 1 to 64.
P Register	Note that if the demo software is not used, the actual number programmed into the register is one less than the desired number. This register stores the value of the lower number for the dual modulus. This is used by the software program only to calculate the desired numbers. For the evaluation board, the number should be 32.

Once the desired parameters for the reference frequency have been entered, either TAB over to the “SET REF” field and press RETURN, use the mouse to click on it or simultaneously press the ALT key and the “r” letter. Note that the Default button returns you to the values seen when first powering up the unit.

6.1.4 Frequency Control

The first data field in the window is the critical field that allows the user to program a desired frequency. Simply enter the desired frequency within the range of 1,600-1,900 MHz with 250 kHz steps into the “Desired Freq” field and the program will automatically calculate the necessary parameters for the chip and display the results in the “Actual Freq” window. Note that it will round off the selected frequency to a valid frequency (i.e., with 250 kHz steps).



SEI-1618EB-00 OPERATING INSTRUCTIONS

Once the desired frequency has been chosen either TAB over to “SET FREQ” field and press ENTER, use the mouse to click the “SET FREQ” field or simultaneously press the ALT key and the “f” letter.

The program does allow the user to change some of the other parameters such as the N, M and K counters. However, if these parameters are changed, the value shown in the “Desired Freq” field will be incorrect but the value shown in the “Actual Freq” field will reflect the changes. If the user wishes to recalculate the N, M, and K counters based on the number entered in the “Desired Freq” field, simple TAB over to the “Re-Compute” field and press RETURN or click on this field with the mouse or simultaneously press the ALT key and the “c”.

You may change the “fixed” parameters such as the R and F registers (external reference frequency and P registers should probably not be changed) as described above but it will then be necessary to “Re-Compute” the desired frequency.

Due to the use of a $\div 32/33$ dual modulus, the minimum divide ratio is 992 ($P \cdot [P-1]$). The reference into the phase detector (determined by the reference divider) determines this division ratio. With the 1600 MHz minimum frequency of the evaluation board and the use of the $\div 32/33$, maximum reference frequency becomes approximately 1.61 MHz. This does not mean that a higher frequency could not be used in this scenario but it does mean that you would not be able to cover the entire range of 1600-1900 MHz with 250 kHz steps. With a larger reference frequency, there would be some frequencies that simply could not be programmed.

Use the mouse to click on the Exit menu to bring up the “Exit to DOS” option and either press RETURN or click on the menu item to exit the program. If keyboard control is desired, simply press the ALT key plus the “x” key and then return to exit the program.

6.2 Other Considerations

There are other windows (output) available with this program that is intended for debugging. If additional information is required, please consult the factory.



7. GLOSSARY OF TERMS

The following section describes the different terms used in the ALL™ architecture (Main Loop). The range of values valid for each parameter and any suggested configuration are given where applicable.

7.1 Reference Frequency

The external reference frequency is supplied to the female SMA connector as indicated in the drawing/photo. This frequency determines the values used in the N, M, and K registers described later. The nominal value is 10.000 MHz.

7.2 Reference Divider (R)

The Reference Divider, R register, determines the actual reference into the digital phase detector. Permissible values for the R register are 2 to 32 (5 binary bits). Although the actual number loaded into the register is one less than the desired number. The R register is set to 8 for the evaluation board.

7.3 Fractionality (F)

The fractionality is the heart of the ALL™ and is what improves the close-in phase noise performance over the performance of a single PLL. Permissible values for the F register are 2 to 64 (6 binary bits) although the actual number loaded into the register is one less than the desired number. In the evaluation board, the fractionality is set to 5.

7.4 Frequency Resolution (step size)

The frequency resolution or step size of the main loop is determined by a combination of the reference frequency, the reference divider (R register), and the selected fractionality, F register. In the evaluation board, the reference into the phase detector is 1.25 MHz so the R register becomes 8. With a fractionality of 5, the frequency step size is therefore calculated as follows:

$$F_{\text{step}} = f_{\text{CLOCK}} \div R \div F \quad (\text{Eq 1})$$

Note that the actual frequency resolution also includes any fixed prescalers ($\div D$) used in the circuit (to bring the output frequency into a range that can be handled by the counters). For the evaluation board, no additional divider is required to reduce the frequency into the dual modulus prescaler ($\div 32/33$). The formula for the step size is therefore modified as follows:

$$F_{\text{step}} = f_{\text{CLOCK}} \div R \div F \cdot D \quad (\text{Eq 2})$$

$$F_{\text{step}} = 10 \text{ MHz} \div 8 \div 5 = 250 \text{ kHz}$$



7.5 Main Divider (N)

The N register determines the number of clocks that the dual modulus will divide by MOD1 (smaller of the two choices for the dual modulus — 32 for the evaluation board). Permissible values for the N register are 8 to 255 (8 binary bits). For the evaluation board, the permissible values are 38 to 46.

Note that the value of the N register ***MUST BE GREATER*** than the value of the M register.

7.6 Modulus Divider (M)

The M register determines the number of clocks that the dual modulus will divide by MOD2 (larger of the two choices for the dual modulus — 33 for the evaluation board). Permissible values for the M register are 0 to 31 (5 binary bits).

7.7 Fractional Divider (K)

The K register controls the smallest steps in the synthesizer by allowing additional divisions by MOD2 (larger of the two choices for the dual modulus — 33 for the evaluation board) within each period determined by the phase detector reference (2.5 MHz in this case). Permissible values for the K register are 0 to 4 (3 binary bits).

7.8 Phase Polarity (PP)

This one bit allows for the electrical switching of the \emptyset_R and \emptyset_V outputs from the phase detector. The outputs of the phase detector (pins 3 and 5) on the SEI-1618PG (U4) will switch with the toggling of this bit. Set this bit to 0.

7.9 Modulus Polarity (MP)

This one bit allows for the electrical switching (polarity) of the modulus control line (pin 10 of the SEI-1618PG). For most dual modulus prescalers, the lower divide number (P) is selected when the modulus control line is HIGH. The Modulus Polarity bit (MP) should be set to LOW (“0”) for these units. Use MP = 1 if the lower divide number (P) is active when the modulus control line (pin 10 on the SEI-1618PG) is LOW.



8.1 LOADING SEQUENCE

The following sequence is used to load the frequency control logic into the evaluation board. Data loading is the MSB first (i.e., K5 is first, K4 is second, K3 is third, etc.). The serial interface contains two registers to allow for infrequently changed parameters such as the polarity bits (PP & MP), Reference Divider (R), and the fractionality (F) to be programmed only once while the data needed to control specific frequency (N, M, and K) can be updated separately.

The last data bit in each sequence is the Control Bit that determines which register is loaded. The control register (Reg 0) is:

↓ First Bit	Control Bit ↓	
MP, PP, R4, R3, R2, R1, R0, F5, F4, F3, F2, F1, F0, 1		Reg 0

The frequency register (Reg 1) is:

↓ First Bit	Control Bit ↓	
K5, K4, K3, K2, K1, K0, M4, M3, M2, M1, M0, N7, N6, N5, N4, N3, N2, N1, N0, 0		Reg 1

In each word (**K0**..K5, **M0**..M4, **F0**..F5, **N0**..N7, **R0**..R4) the least significant bit (LSB) of each word is indicated above by the bold and underlined term.

This bit stream is applied to pin 2 (Serial Data) of the 25-pin subminiature connector (P1). The Serial Clock line (pin 5) is used to load the above data into the internal registers on the rising edge of each clock until all of the data is shifted into the registers. The maximum clock rate is 1 MHz. Once the data has been loaded into the registers, the Serial Latch (pin 6) is used to transfer the data from the registers to the counters and produces the desired output frequency. Note that an extra data shift can occur if extra clocks are present after the Serial Latch (pin 6) is sent. There are two ways to prevent this from occurring. If the Serial Clock is removed from Pin 5 after the last data bit is sent and before the Serial Latch completes its high to low transition, no extra data shift will occur. Alternatively, if the Serial Latch remains at a TTL High after the low to high transition, no additional data will be shifted into the registers.

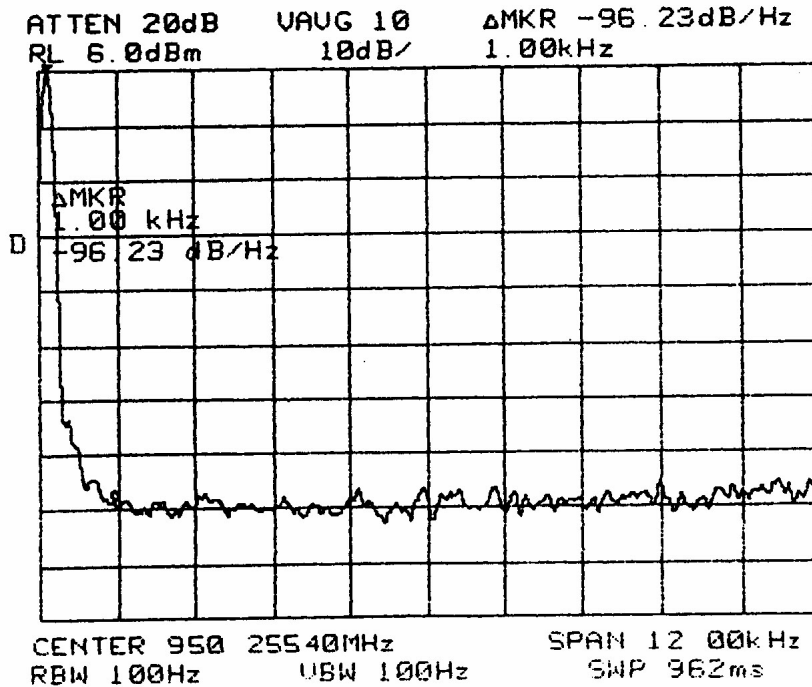
Remember that the loop parameters have been optimized for 250 kHz steps. Other step sizes are possible with the software but the spurious response and/or the phase noise may degrade as a result.



9. COMPARISON — Single PLL vs ALL™

The figure below (Figure 3) illustrates typical performance with a traditional single PLL operating at 900 MHz with 50 kHz steps. With this step size, the division ratio becomes roughly 18,000 which is 85 dB degradation of the phase within the loop bandwidth ($20 * \log [\text{division ratio}]$). In the single PLL circuit, the phase noise is approximately -65 dBc/Hz.

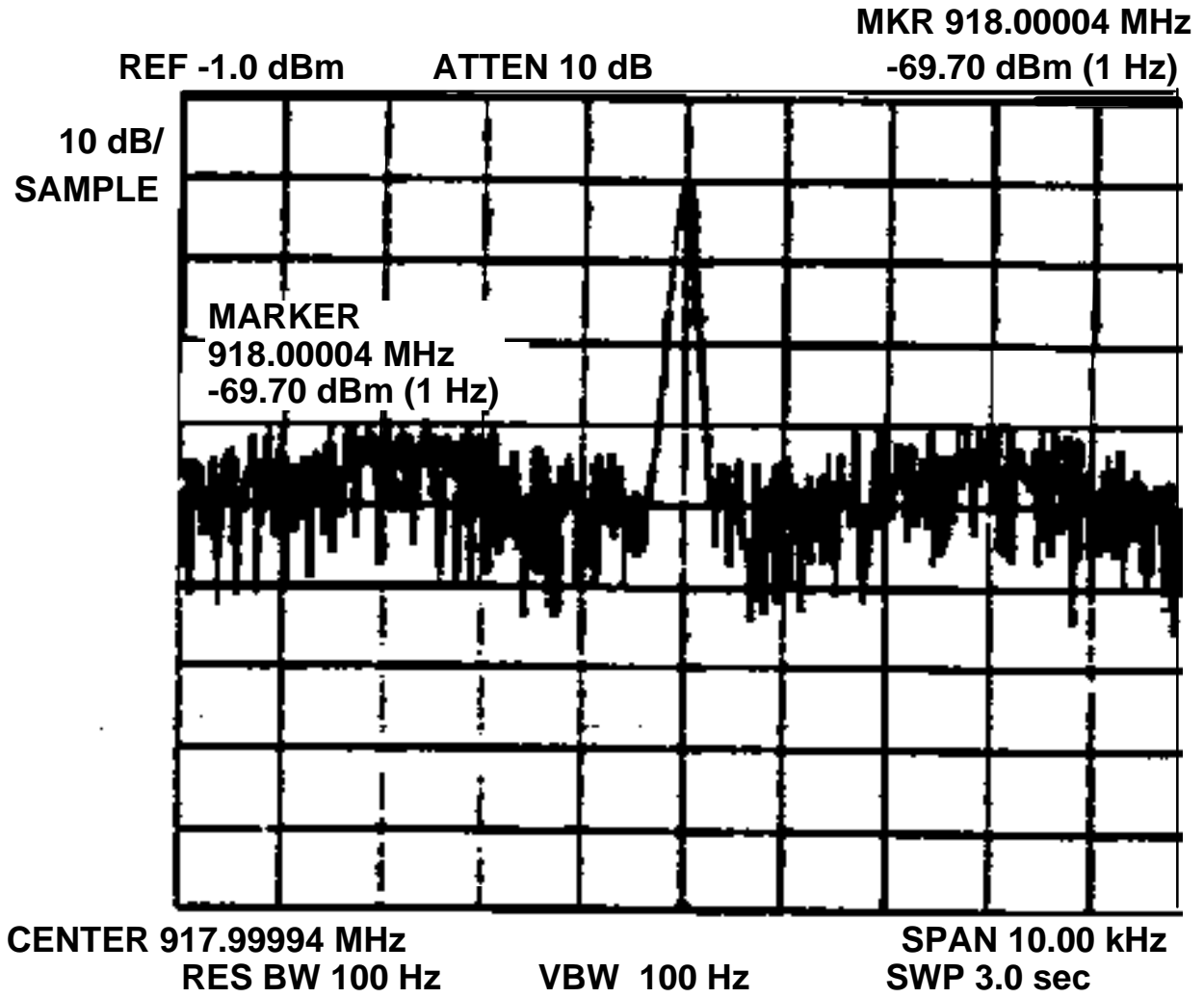
Measure the phase noise of the ALL™ circuit and you will notice that the performance is better. Now count the number of VCOs and you will find out that only one loop is used as well. The addition of the ALL™ architecture allows the use of a higher reference into the phase detector (1.25 MHz) while still maintaining the same step size of 50 kHz by programming a fractionality of 25.



Phase Noise Plot — SEI-1618EB-00



SEI-1618EB-00 OPERATING INSTRUCTIONS

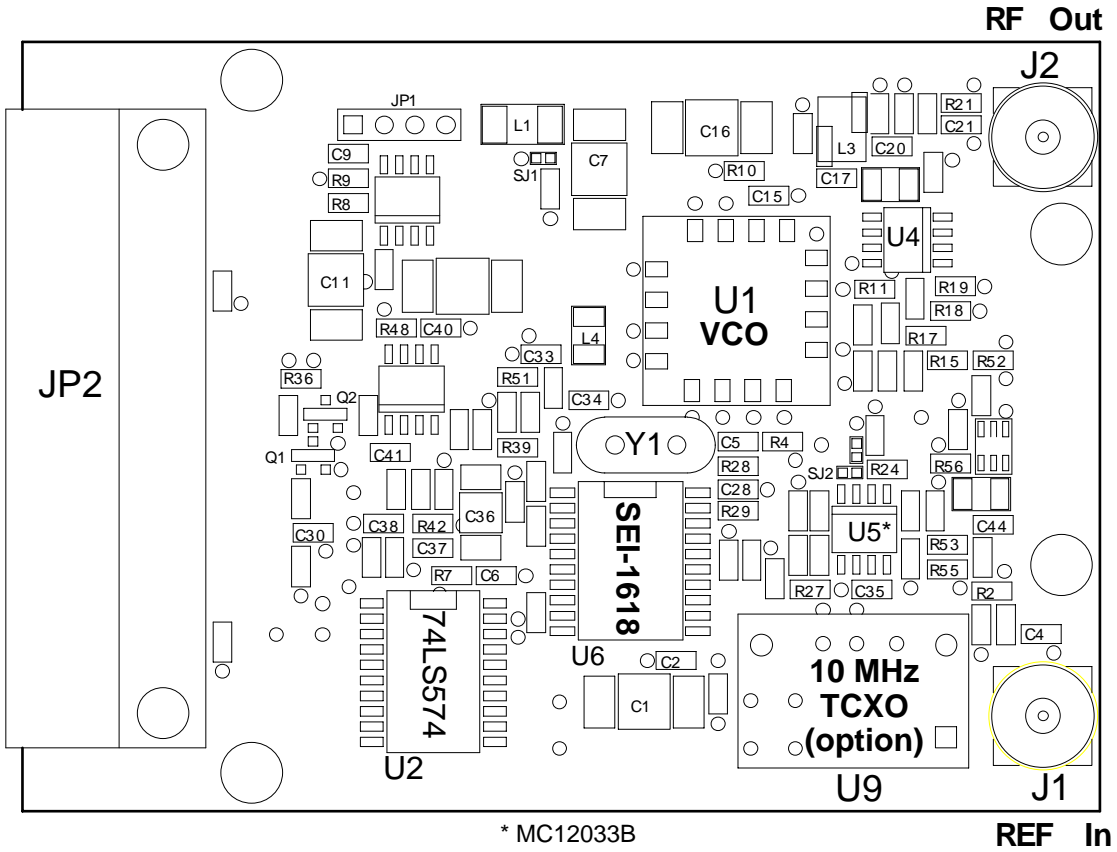


Phase Noise Plot — Non-Fractional PLL



SEI-1618EB-00 OPERATING INSTRUCTIONS

10. Board Layout



Component Side — SEI-1618EB-00



SEI-1618EB-00 OPERATING INSTRUCTIONS

11. ALARM (Lock Indicator)

Pin 3 of the 4-pin IDC header contains the lock indicator control line. This line provides access to the status of the PLL loop. The signal is a TTL level voltage. The following table contains the Logic State for Lock/Out-of-Lock indication.

INDICATION	LOCK LINE LEVEL
PLL Locked	TTL LOW
PLL Out-of-Lock	TTL HIGH

Lock Indicator Logic

12. WARRANTY

All Meret products are warranted against defects in material and workmanship for a period of one year after initial shipment. Meret will repair or replace any circuit or component that is found to be defective during this period if in Meret's sole opinion the product is deemed defective.

Any modifications or options performed by Meret during the initial one-year period shall be included under the initial warranty, and such secondary warranties shall terminate one year after the initial shipment. Shipment of the product to Meret (San Diego, CA) shall be made prepaid and shall not be made without prior authorization by Meret.

This warranty is voided if the product is abused or if the user makes unauthorized modifications.

This warranty is in lieu of all other warranties, expressed or implied, and no person is authorized to represent or assume for Meret any liability in connection with the sales of our products other than stated within this warranty.

Serial Number

QC by _____ Date: _____

