

# OPERATING INSTRUCTIONS

## VDS-2700-1137 UHF Frequency Synthesizer

### 1. PRODUCT DESCRIPTION

The VDS-2700-1137 is a serially controlled frequency synthesizer designed to operate from 700 MHz to 830 MHz with <1 kHz steps. This unit is based on our VDS-6000 family of Phase Lock Loop (PLL) synthesizers that combines our unique patent pending Arithmetic Lock Loop (ALL) design with a Direct Digital Synthesizer (DDS) for fine resolution at higher frequencies than can be achieved by DDS products alone. The ALL section covers the overall operating range of the unit in 625 kHz steps and the DDS circuitry adds the remaining resolution. Due to the frequency range, the use of the ALL circuitry improves the close-in phase noise performance by about 10 dB over a traditional single loop design while maintaining a cost effective solution.

### 2. PERFORMANCE/SPECIFICATIONS

#### Frequency

Range .....	700 MHz to 830 MHz
Resolution.....	1 kHz
Control (ALL).....	30 bits, Serial Binary Positive-true TTL logic
Control (DDS) .....	32 bits, Serial Binary Positive-true TTL logic

#### Main Output

Level .....	+8 dBm into 50 $\Omega$
Flatness .....	$\pm 2$ dB

#### Spectral Purity

Harmonics.....	<-35 dBc
Spurious (within band of 600 MHz to 930 MHz)	
	<-40 dBc (<10 kHz)
	<-60 dBc (>10 kHz)

#### Phase Noise

100 Hz offset.....	<-65 dBc/Hz
1 kHz offset.....	<-80 dBc/Hz
10 kHz offset.....	<-93 dBc/Hz
100 kHz offset.....	<-105 dBc/Hz



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### 2. PERFORMANCE/SPECIFICATIONS (continued)

**Frequency Ref** ..... 10.000 MHz External  
 Level ..... 0 dBm  $\pm$ 3 dB  
**Lock Indicator** ..... TTL High for Lock; Low for Out-of-Lock

#### Connectors

REF In ..... SMA female (J1)  
 REF Out ..... SMA female (J2) — optional  
 RF Out ..... SMA female (J3)  
 Freq Control ..... 9-pin subminiature “D” (P1) — male  
 Power Supply ..... same as frequency control

**Power Supply** ..... +5V @ 500 mA; +12V @ 250 mA (max)

#### Environmental

Operating Temp ..... 0°C to +50°C  
 Storage Temp ..... -20°C to +70°C  
 Dimensions ..... 3.5” x 4.77” x 0.9”  
 Weight ..... <1 lbs, net; 4 lbs, shipping

### 3. MECHANICAL CONFIGURATION

The VDS-2700-1137 is manufactured in a single module with a 9-pin (male) connector and the 10 MHz REF In SMA female (J1) and RF Out SMA female (J3) located on the 3.5” x 0.9” face. The following table describes each of the inputs and outputs:

Designator	Function	Connector	Mating Connector
J1	10 MHz REF In	SMA female	SMA male
J2	10 MHz REF Out	SMA female-optional	SMA male
J3	RF Out	SMA female	SMA male
P1	Frequency Control	9-pin Submini “D” male	Amphenol 117DE-9S or equivalent



**4. POWER SUPPLY CONNECTIONS**

Power is supplied to the following pins on the 9-pin subminiature “D” connector:

Power Supply	Pin Numbers
+5V	1
+12V	6
GND	5

**5. FREQUENCY CONTROL**

All control lines should be driven with standard CMOS levels ("0" = 0V to 0.4V for "low" and "1" =2.4V to 5.5V for "high".) The VDS-2700-1137 is configured for serial frequency control only.

PIN NO.	NAME	DESCRIPTION
1	+5V dc	Bias Voltage
2	P Lock	Lock Indicator (Low = Out of Lock)
3	Serial Latch	Latch for Coarse Steps (main loop)
4	Serial Latch1	Latch for fine steps (DDS)
5	GND	Ground Return
6	+12V dc	Bias Voltage
7	Serial Clock	Clock used for both data words
8	Serial Data	Data word for Coarse Steps (main loop)
9	Serial Data1	Data word for Fine Steps (DDS)

Pin Assignments (P1)

**6. GLOSSARY OF TERMS**

The following section describes the different terms used in the ALL™ architecture (Main Loop). The range of values valid for each parameter and any suggested configuration are given where applicable.

**6.1 Reference Frequency**

The external reference frequency is supplied to the female SMA connector (J1). This frequency determines the values used in the N, M, and K registers described later. The nominal value is 10.000 MHz.

**6.2 Reference Divider (R)**



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The Reference Divider, R register, determines the actual reference into the digital phase detector. Permissible values for the R register are 2 to 32 (5 binary bits) although the actual number loaded into the register is one less than the desired number. The R register is set to 3 (4-1) for the VDS-2700-1137.

### 6.3 Fractionality (F)

The fractionality is the heart of the ALL™ and is what improves the close-in phase noise performance over the performance of a single PLL. Permissible values for the F register are 2 to 16 (4 binary bits) although the actual number loaded into the register is one less than the desired number. In the VDS-2700-1137, the fractionality is set to 16 by loading the F register with 15 (16-1).

### 6.4 Frequency Resolution (step size)

The frequency resolution or step size of the main loop is determined by a combination of the reference frequency, the reference divider (R register), and the selected fractionality, F register. In the VDS-2700-1137, the reference into the phase detector is 2.5 MHz so the R register becomes 4. With a fractionality of 16, the frequency step size is therefore calculated as follows:

$$F_{\text{step}} = f_{\text{CLOCK}} \div R \div F \quad (\text{Eq 1})$$

Note that the actual frequency resolution also includes any fixed prescalers ( $\div D$ ) used in the circuit (to bring the output frequency into a range that can be handled by the counters). For the VDS-2700-1137, a fixed divide-by-4 ( $\div 4$ ) is used to reduce the frequency into the dual modulus prescaler ( $\div 5/6$ ). The formula for the step size is therefore modified as follows:

$$F_{\text{step}} = f_{\text{CLOCK}} \div R \div F \cdot D \quad (\text{Eq 2})$$

$$F_{\text{step}} = 10 \text{ MHz} \div 4 \div 16 \cdot 4 = 625 \text{ kHz}$$

### 6.5 Main Divider (N)

The N register determines the number of clocks that the dual modulus will divide by MOD1 (smaller of the two choices for the dual modulus — 5 for the VDS-2700-1137). Permissible values for the N register are 8 to 255 (8 binary bits). For the VDS-2700-1137, the permissible values are 13 to 16.



Note that the value of the N register ***MUST BE GREATER*** than the value of the M register.

### 6.6 Modulus Divider (M)

The M register determines the number of clocks that the dual modulus will divide by MOD2 (larger of the two choices for the dual modulus — 6 for the VDS-2700-1137). Permissible values for the M register are 0 to 4 (4 binary bits).

### 6.7 Fractional Divider (K)

The K register controls the smallest steps in the synthesizer by allowing additional divisions by MOD2 (larger of the two choices for the dual modulus — 6 for the VDS-2700-1137) within each period determined by the phase detector reference (2.5 MHz in this case). Permissible values for the K register are 0 to 15 (4 binary bits).

### 6.8 Phase Polarity (P)

This one bit allows for the electrical switching of the  $\Phi_V$  and  $\Phi_R$  outputs from the phase detector. The outputs of the phase detector (pins 31 and 37) on the PLD containing the ALL™ circuitry (U4) will switch with the toggling of this bit. Set this bit to 0.

### 6.9 T Register

This function is not used at this time. Permissible values for the T register are 0 to 15 (4 binary bits) but to avoid extraneous results, a value of zero (0) must be loaded into the register.

## 7.1 LOADING SEQUENCE — ALL™ (Main Loop)

The following sequence is used to load the frequency control logic into the VDS-2700-1137. Data loading is first bit in to last bit in (i.e., K3 is first, K2 is second, K1 is third, etc.).

K3, K2, K1, K0, M3, M2, M1, M0, T3, T2, T1, T0, F3, F2, F1, F0,  
N7, N6, N5, N4, N3, N2, N1, N0, R4, R3, R2, R1, R0, P.

In each word (**K0**..K3, **M0**..M3, **T0**..T3, **F0**..F3, **N0**..N7, **R0**..R4) the least significant bit (LSB) of each word is indicated above by the bold and underlined term.



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This bit stream is applied to pin 8 (Serial Data) of the 9-pin subminiature connector (P1). The Serial Clock line (pin 7) is used to load the above data into the internal registers on the rising edge of each clock until all of the data is shifted into the registers. The maximum clock rate is 1 MHz. Once the data has been loaded into the registers, the Serial Latch (pin 3) is used to transfer the data from the registers to the counters and produces the desired output frequency. Note that an extra data shift can occur if extra clocks are present after the Serial Latch (pin 3) is sent. There are two ways to prevent this from occurring. If the Serial Clock is removed from Pin 7 after the last data bit is sent and before the Serial Latch completes its high to low transition, no extra data shift will occur. Alternatively, if the Serial Latch remains at a TTL High after the low to high transition, no additional data will be shifted into the registers.

### 7.2 LOADING SEQUENCE — DDS (Fine Loop)

The control word for the DDS is 32 bits. This data is loaded into the synthesizer with the Serial Data1 line (pin 9) with the MSB sent first. The range for allowable values of the DDS is 156.25 kHz to 312.25 kHz. The nominal step size is 250 Hz which will cause the output to change by the desired 1 kHz (due to the fixed ÷4 prescaler used to reduce the frequency into the dual modulus).

The DDS is clocked by the reference frequency of 10 MHz and has 32 bits of resolution. The frequency will be loaded into the DDS on the rising edge of Serial Latch1.

The DDS is programmed as a binary number according to the formula:

$$F_{\text{DDS}} = \frac{10 \text{ MHz}}{2^{32}} \cdot F$$

where F is an integer between 67108864 (400 0000<sub>H</sub>) and 134217728 (800 0000<sub>H</sub>),

## 8. DESIRED FREQUENCY CALCULATION

The desired frequency for the main loop (ALL™) is programmed through the three registers — N, M, and K. The final output frequency is a combination of the Main loop (ALL) and the DDS.

The three ALL™ registers drive the dual modulus so the formula describing the method of calculating these registers is dependent on the dual modulus selected. In the VDS-2700-1137, a ÷5/6 dual modulus is used. Note that valid frequencies for the VDS-2700-1137 fall between 700 MHz and 830 MHz.



The general formula for calculating the desired output frequency is:

$$f_{ALL} = \frac{\text{Reference Frequency}}{R} \cdot \left\{ \text{MOD2} \cdot M + \text{MOD1} \cdot (N - M) + \frac{K}{F} \right\} \cdot D \quad (\text{Eq 3a})$$

$$f_{\text{fine}} = (f_{\text{DDS}} - 0.15625) \cdot D \quad (\text{Eq 3b})$$

$$f_{\text{out}} = f_{ALL} + 4 \cdot f_{\text{DDS}} = f_{ALL} + f_{\text{fine}} + 0.625 \text{ MHz} \quad (\text{Eq 3c})$$

$$f_{\text{fine}} = f_{\text{out}} - f_{ALL} - 0.625 \text{ MHz} \quad (\text{Eq 3d})$$

$$= (f_{\text{out}} - 0.625) - \frac{\text{Ref Freq}}{R} \cdot \left\{ \text{MOD2} \cdot M + \text{MOD1} \cdot (N - M) + \frac{K}{F} \right\} \cdot D \quad (\text{Eq 3e})$$

- Where:
- MOD1 = Lower dual modulus value (in VDS-SP-1148 = 5)
  - MOD2 = Higher dual modulus value (in VDS-SP-1148 = 6)
  - N = N Register value (Main counter)
  - M = M Register value (modulus counter)
  - K = K Register value (fractional value)
  - F = F Register value (fractionality)
  - R = R Register value (reference divider)
  - $f_{\text{DDS}}$  = Programmed DDS Frequency (in MHz)
  - $f_{\text{fine}}$  = Effective DDS Frequency inside Main Loop
  - $f_{\text{out}}$  = Desired Frequency (in MHz)
  - 0.625 MHz = Offset so that programming DDS portion of the synthesizer at the minimum value (156.25 kHz) results in no contribution to output frequency.

For the VDS-2700-1137, the formula becomes:

$$f_{ALL} = \frac{\text{Reference Frequency}}{4} \cdot \left\{ 6 \cdot M + 5 \cdot (N - M) + \frac{K}{16} \right\} \cdot 4 \quad (\text{Eq 4a})$$

and

$$f_{\text{out}} (\text{MHz}) = 4 \cdot \left\{ 2.5 \cdot (M + 5 \cdot N + \frac{K}{16}) + f_{\text{DDS}} \right\} \quad (\text{Eq 5})$$



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As the K value increments, the output will change by 625 kHz. The DDS fills in this 625 kHz steps since it covers 156.25 kHz to 312.225 kHz (bandwidth  $\approx$ 156.25 kHz) in 250 Hz steps. The use of the divide-by-4 prescaler effectively multiplies this by 4 so the actual bandwidth covered is 625 kHz. The N & M values are calculated as follows:

The amount of division needed to lock the desired frequency is calculated as the frequency presented to the main counter (desired frequency divided by 4, the fixed prescaler D), the DDS offset, plus the additional division due to the reference frequency into the phase detector (2.5 MHz).

The N value is calculated as the integer of this resulting number divided by the smaller modulus value (5).

The M value is then calculated as the integer portion of the fractional part of this remainder times the smaller modulus value (5) divided by the smaller modulus value (5).

Finally, the K value is calculated as the fractional part of the M value times the fractionality (16).

These calculations are given by the following formulas:

$$N_T = \left\{ \frac{(f_{out} - 0.625 \text{ MHz}) \div 4}{2.5 \text{ MHz}} \right\} = \frac{(f_{out} - 0.625 \text{ MHz})}{10 \text{ MHz}} \quad (\text{Eq. 6})$$

$$N = \text{INT} \left\{ \frac{N_T}{5} \right\} \quad (\text{Eq. 7})$$

$$M = \text{INT} \left\{ \left( \frac{N_T}{5} - N \right) \cdot 5 \right\} = \text{INT} \left\{ \text{Frac} \left( \frac{N_T}{5} \right) \cdot 5 \right\} \quad (\text{Eq. 8})$$

$$K = \text{INT} \left[ 16 \cdot \text{Frac} \left\{ \text{Frac} \left( \frac{N_T}{5} \right) \cdot 5 \right\} \right] \quad (\text{Eq. 9})$$

$$f_{fine} = (f_{out} - 0.625) - 10 \cdot \left\{ M + 5 \cdot N + \frac{K}{16} \right\} \quad (\text{Eq. 10})$$

From equation 3b, we can derive  $f_{DDS}$  as follows:



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$$f_{\text{DDS}} = \frac{f_{\text{fine}}}{D} + 0.15625 \quad (\text{Eq. 11})$$

Note that equation 6 gives the total divide ratio for the synthesizer.

### 9. PROGRAMMING EXAMPLES

Use equations 6-10 to calculate the necessary values to program the synthesizer:

Several examples will be presented to assist the user in determining the values needed for each register. Note that the F Register is always set to 16 and the R Register is always set to 4 and have been omitted from the table.

DESIRED FREQUENCY	REGISTERS			DDS OFFSET (kHz)	f <sub>DDS</sub> (kHz)
	N	M	K		
700.000 MHz	13	4	15	000	156.250
775.532 MHz	15	2	7	532	289.250
799.999 MHz	15	4	14	624	312.250
800.000 MHz	15	4	15	000	156.250
829.998 MHz	16	2	14	623	312.000
829.999 MHz	16	3	14	624	312.250
830.000 MHz	16	3	15	000	156.250

### 10. ALARM (Lock Indicator)

Pin 2 of the 9-pin subminiature “D” connector (J1) contains the lock indicator control line. This line provides access to the status of the PLL loop. The signal is a TTL level voltage. The following table contains the logic state for Lock/Out-of-Lock indication. A red LED is also provided to allow visual indication of a Out-Of-Lock condition.

INDICATION	LOCK LINE LEVEL
Synthesizer Locked	TTL High
Synthesizer Out-of-Lock	TTL Low

Lock Indicator Logic



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**11. WARRANTY**

All Meret products are warranted against defects in material and workmanship for a period of one year after initial shipment. Meret will repair or replace any circuit or component that is found to be defective during this period if in Meret's sole opinion the product is deemed defective.

Any modifications or options performed by Meret during the initial one year period shall be included under the initial warranty, and such secondary warranties shall terminate one year after the initial shipment. Shipment of the product to Meret (San Diego, CA) shall be made prepaid and shall not be made without prior authorization by Meret.

This warranty is voided if the product is abused or if unauthorized modifications are made by the user.

This warranty is in lieu of all other warranties, expressed or implied, and no person is authorized to represent or assume for Meret any liability in connection with the sales of our products other than stated within this warranty.

\_\_\_\_\_  
Serial Number

QC by \_\_\_\_\_ Date: \_\_\_\_\_

