OPERATING INSTRUCTIONS

VDS-6501-1238 L-band Frequency Synthesizer

1. PRODUCT DESCRIPTION

The VDS-6501-1238 is a parallel controlled frequency synthesizer designed to operate from 1,850 MHz to 2,100 MHz with 250 kHz steps. This unit is based on our VDS-6000 family of Phase Lock Loop (PLL) synthesizers that combines a traditional PLL with a unique patented Arithmetic Lock Loop (ALL) design. The PLL section covers the overall operating range of the unit in 5 MHz steps and the ALL circuitry adds the remaining resolution. Due to the frequency range, the use of the ALL circuitry improves the close-in phase noise performance by 26 dB over a traditional single loop design while maintaining a cost effective solution.

In addition, the "-1238" has been designed to use our custom PLD to reduce circuitry further and permit either serial or parallel control.

2. PERFORMANCE/SPECIFICATIONS

Frequency
- Range .....1,850 MHz to 2,100 MHz
- Resolution.....250 kHz
- Control .....13 bits, parallel Binary Positive-true TTL logic

Main Output (J)
- Level .....+10 dBm into 50?
- Flatness .....±2 dB

Spectral Purity
- Harmonics.....<-30 dBc
- Spurious .....<-60 dBc
  - 1 kHz offset.....<-60 dBc/Hz
  - 10 kHz offset.....<-90 dBc/Hz

Frequency Ref .....10.000 MHz Internal
- Accuracy .....±1 ppm/year
- Output .....>-15 dBm

Lock Indicator.....TTL LOW for Lock; TTL HIGH for Out-of-Lock

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2. PERFORMANCE/SPECIFICATIONS (continued)

Connectors

REF Out .....SMA female (J2)
RF Out .....SMA female (J1)
Freq Control.....25-pin subminiature "D" (P1) — male
Power Supply.....9-pin subminiature "D" (P2) — male

Power Supply .....+5V @ 300 mA (max); +24V @ 130 mA (max)

Environmental

Operating Temp.....0°C to +50°C
Storage Temp.....-20°C to +70°C
Dimensions .....4.48" x 6.6" x 1.125"
Weight.....<2 lbs, net; 6 lbs, shipping

3. MECHANICAL CONFIGURATION

The VDS-6501-1238 is manufactured in a single module with all connectors — 25-pin (male) connector, 9-pin (male) connector, RF Out (J1) and the 10 MHz REF Out SMA (J2) located on the 6.6"" x 1.125" face with the following table describing each of the inputs and outputs:

Designator	Function	Connector	Mating Connector
P1	Frequency Control	25-pin Submini "D" male	Amphenol 117DB-25S or equivalent
P2	Power Supply	9-pin Submini "D" male	Amphenol 117DE-9S or equivalent
J1	RF Out	SMA female	SMA male
J2	10 MHz REF Out	SMA female	SMA male

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4. POWER SUPPLY CONNECTIONS (P2)

Power is supplied to the following pins on the 9-pin subminiature "D" connector:

Power Supply	Pin Numbers
+5V	3, 8
+24V	2, 7
GND	1, 6

Power Supply Pin Assignments (P2)

5. FREQUENCY CONTROL (P1)

All control lines should be driven with standard TTL levels ("0" = 0V to 0.4V for "low" and "1" =2.4V to 5.5V for "high".) The VDS-6501-1238 is configured for parallel frequency control only. Note that it is possible to re-configure the unit for serial loading by changing internal solder jumpers. Consult the factory for more details.

Pin No.	Description	Pin No.	Description	Pin No.	Description
1	GND	**9**	K0	**18**	N6*
2	Lock Ind	**10**	K2	**19**	M0
3	N1	**11**	K4	**20**	M2
4	N3	**12**	K6*	**21**	M4*
5	N5*	**13**	GND	**22**	K1
6	N7*	**14**	GND	**23**	K3
7	M1	**15**	N0	**24**	K5*
8	M3	**16**	N2	**25**	K7*
		17	N4**		

Frequency Control Pin Assignments (P2)

* May be permanently tied to ground by the user for this frequency range so that the total number of bits for control is reduced.

** Always TTL "1" for this frequency range. Signal is tied to a pull up resistor so no connection is necessary.

6. GLOSSARY OF TERMS

The following section describes the different terms used in the ALL™ architecture. The range of values valid for each parameter and any suggested configuration are given where applicable.

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6.1 Reference Frequency (F_{ref})

The internal reference frequency is supplied to the female SMA connector (J). This frequency determines the values used in the N, M, and K registers described later. The nominal value is 10.000 MHz.

6.2 Reference Divider (R)

The Reference Divider, R register, determines the actual reference into the digital phase detector. Permissible values for R are 2 to 32 (5 binary bits) although the actual number loaded into the R register is one less than the desired number. The VDS-6501-1238 is hardwired internally for R = 4 (2.5 MHz).

6.3 Fractionality (F)

The fractionality is the heart of the ALL™ and is what improves the close-in phase noise performance over the performance of a single PLL. Permissible values for F are 2 to 256 (8 binary bits) although the actual number loaded into the F register is one less than the desired number. In the VDS-6501-1238, the fractionality, F, is set to 20.

6.4 Frequency Resolution (step size)

The ultimate frequency resolution or step size is determined by a combination of the reference frequency, the reference divider (R), and the selected fractionality, F. In the VDS-6501-1238, the reference into the phase detector is 2.5 MHz with the R register at 3 (4-1). Note that the actual frequency resolution also includes any fixed prescalers (÷D) used in the circuit. With a fractionality of 20, the frequency step size is therefore calculated as follows:

$$\mathbf{F}_{step} = \boldsymbol{f}_{REF} \div R \div F \bullet D \qquad \text{(Eq 1)}$$

For the VDS-6501-1238, the S-band output, 1,850 MHz to 2,100 MHz, is first divided by 2 so that the highest frequency presented to the dual modulus (÷16/17) is less than its upper limit. Thererfore, the step size is therefore calculated as follows:

$$\mathbf{F}_{step} = 10 \text{ MHz} \div 4 \div 20 \bullet 2 = 250 \text{ kHz}$$

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6.5 Main Divider (N)

The N register determines the number of clocks that the dual modulus will divide by MOD1 (smaller of the two choices for the dual modulus — 16 for the VDS-6501-1238). Permissible values for the N register are 10 to 255 (8 binary bits). Only 4 bits are needed for the VDS-6501-1238 plus one bit that is always high.

> Note that the value of the N register ***MUST BE GREATER*** than the value of the M register in order to generate all contiguous division ratios over the band.

6.6 Modulus Divider (M)

The M register determines the number of clocks that the dual modulus will divide by MOD2 (larger of the two choices for the dual modulus — 17 for the VDS-6501-1238). Permissible values for the M register are 0 to 31 (5 binary bits). Only 4 bits are needed for the VDS-6501-1238.

6.7 Fractional Divider (K)

The K register controls the smallest steps in the synthesizer by allowing additional divisions by MOD2 (larger of the two choices for the dual modulus — 17 for the VDS-6501-1238) within each period determined by the phase detector reference (2.5 MHz in this case). Permissible values for the K register are 0 to 255 (8 binary bits) but in the VDS-6501-1238, this is further limited to 5 bits (0 - 31).

6.8 Phase Polarity (P)

This one bit allows for the electrical switching of the Φ_V and Φ_R outputs from the phase detector. The outputs of the phase detector (pins 31 and 37) on the PLD containing the ALL™ circuitry (U1) will switch with the toggling of this bit. This bit is hardwired to 0.

6.9 T Register

This function is not used at this time. Permissible values for the T register are 0 to 15 (4 binary bits) but to avoid extraneous results, a value of zero (0) is hardwired on the VDS-6501-1238.

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7. DESIRED FREQUENCY CALCULATION

The desired frequency is programmed through the three registers — N, M, and K. These registers drive the dual modulus so the formula describing the method of calculating these registers is dependent on the dual modulus selected. In the VDS-6501-1238, a ÷16/17 dual modulus is used. Note that valid frequencies for the VDS-6501-1238 fall between 1,850 MHz and 2,100 MHz.

The general formula for calculating the desired output frequency is:

$$f_{out} = D \bullet \frac{\text{Reference Frequency}}{R} \bullet \left\{ MOD2 \bullet M + MOD1 \bullet (N - M) + \frac{K}{F} \right\} \quad \text{(Eq 2)}$$

Where: MOD1 = Lower dual modulus value (in VDS-6501-1238 = 16)
MOD2 = Higher dual modulus value (in VDS-6501-1238 = 17)
N = N Register value (Main counter)
M = M Register value (modulus counter)
K = K Register value (fractional value)
F = F value (fractionality)
R = R value (reference divider)
D = D Value (prescaler) — fixed value of 2 on this product.

For the VDS-6501-1238, the formula becomes:

$$f_{out} = D \bullet \frac{\text{Reference Frequency}}{4} \bullet \left\{ 17 \bullet M + 16 \bullet (N - M) + \frac{K}{20} \right\} \quad \text{(Eq 3)}$$

Which simplifies to:

$$f_{out} = 5 \bullet \left\{ M + 16 \bullet N + \frac{K}{20} \right\} \quad \text{(Eq 4)}$$

As the K value increments by 1, the output will change by 250 kHz.

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The N & M values are calculated as follows:

The amount of division needed to lock the desired frequency is calculated as the frequency presented to the main counter (desired frequency divided by 2 fixed prescaler, ÷D), plus the additional division due to the reference frequency into the phase detector (2.5 MHz).

The N value is calculated as the integer of this resulting number divided by the smaller modulus value (16).

The M value is then calculated as the integer of this remainder times the smaller modulus value (16).

Finally, the K value is calculated as the fractional part of the M value times the fractionality.

These calculations are given by the following formulas:

$$\text{Temp} = \left\{ \frac{f_{\text{desired}}}{2.5\ \text{MHz} \bullet 2} \right\} \qquad \text{(Eq. 5)}$$

$$\text{N} = \text{INT} \left\{ \frac{\text{Temp}}{16} \right\} \qquad \text{(Eq. 6)}$$

$$\text{M} = \text{INT} \left\{ \left(\frac{\text{Temp}}{16} - \text{N} \right) \bullet 16 \right\} = \text{INT} \left\{ \text{Frac} \left(\frac{\text{Temp}}{16} \right) \bullet 16 \right\} \qquad \text{(Eq. 7)}$$

$$\text{K} = 20 \bullet \text{Frac} \left\{ \text{Frac} \left(\frac{\text{Temp}}{16} \right) \bullet 16 \right\} \qquad \text{(Eq. 8)}$$

8. PROGRAMMING EXAMPLES

Several examples will be presented to assist the user in determining the values needed for each register.

DESIRED FREQUENCY	REGISTERS				
	N	M	K	F	R
1,850.000 MHz	23	2	0	20	4
1,850.250 MHz	23	2	1	20	4
1,854.750 MHz	23	2	19	20	4
1,855.000 MHz	23	3	0	20	4
1,999.750 MHz	24	15	19	20	4
2,099.500 MHz	26	3	18	20	4
2,099.750 MHz	26	3	19	20	4
2,100.000 MHz	26	4	0	20	4

9. ALARM (Lock Indicator)

Pin 2 of the 25-pin subminiature "D" connector (P2) contains the lock indicator control line. This line provides access to the status of the PLL loop. The following table contains the logic state for Lock/Out-of-Lock indication. Note that the red LED located beside the J1 connector will illuminate for a OUT-OF-LOCK condition.

INDICATION	LOCK LINE LEVEL
PLL Locked	TTL LOW
PLL Out-of-Lock	TTL HIGH

Lock Indicator Logic

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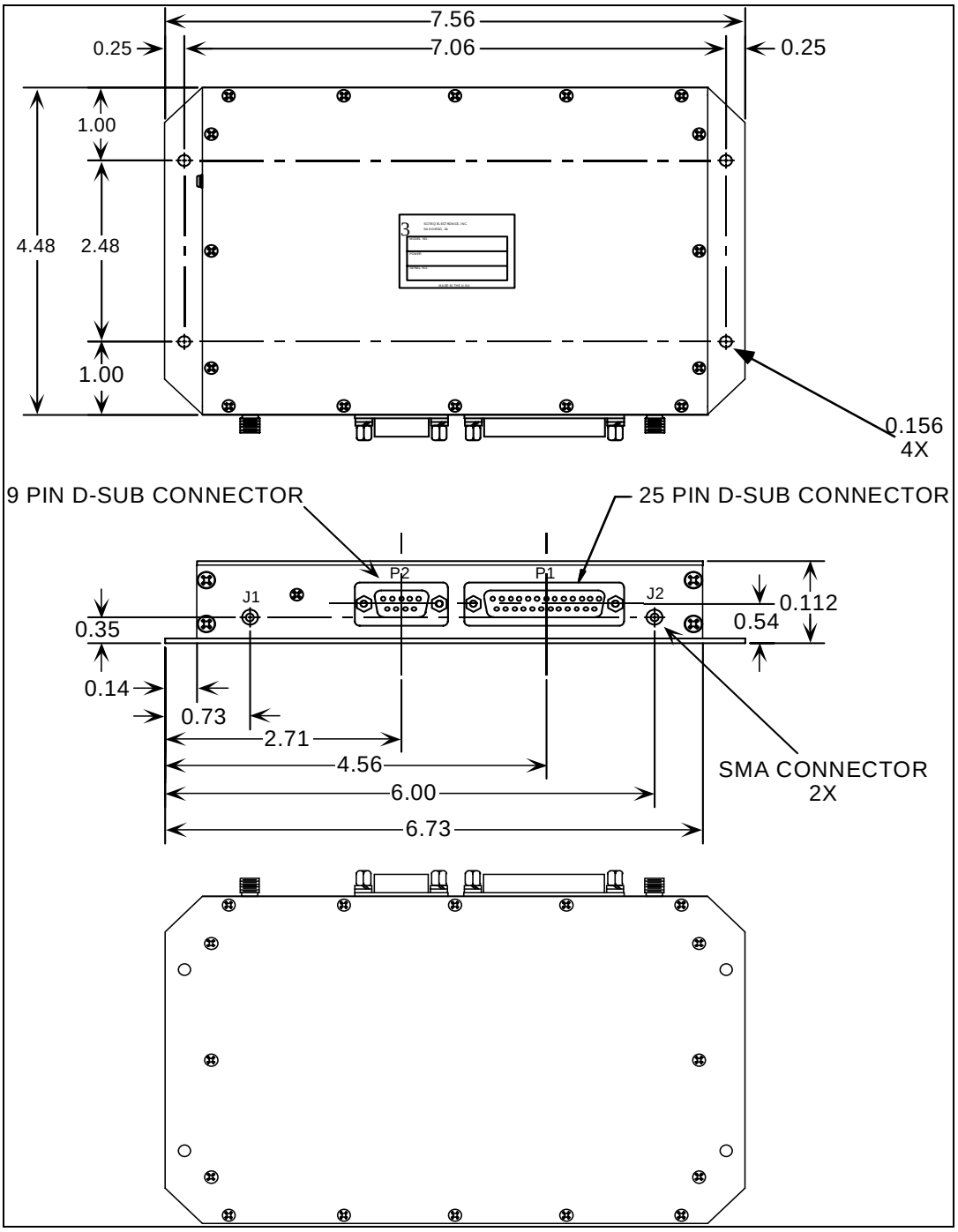

VDS-6501 Outline Drawing

10. WARRANTY

All Meret products are warranted against defects in material and workmanship for a period of **one year** after initial shipment. Meret will repair or replace any circuit or component that is found to be defective during this period if in Meret's sole opinion the product is deemed defective.

Any modifications or options performed by Meret during the initial one year period shall be included under the initial warranty, and such secondary warranties shall terminate one year after the initial shipment. Shipment of the product to Meret (San Diego, CA) shall be made prepaid and shall not be made without prior authorization by Meret.

This warranty is voided if the product is abused or if unauthorized modifications are made by the user.

This warranty is in lieu of all other warranties, expressed or implied, and no person is authorized to represent or assume for Meret any liability in connection with the sales of our products other than stated within this warranty.

_____

_____
Serial Number

QC by _____ Date: _____

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