

OPERATING INSTRUCTIONS

VDS-6600-1436 Fractional PLL Synthesizer

1. PRODUCT DESCRIPTION

The VDS-6600-1436 Fractional Frequency Synthesizer is a state-of-the-art synthesizer module that uses our new device, the SEI-1618PG that contains our patented ALL™ technology for phase noise improvement. The ALL™ is a Meret patented fractional PLL circuit, and is fully programmable — i.e., both the counters AND THE FRACTIONALITY. The VDS-6600-1436 has been customized to provide the desired frequency output of 1,850 MHz to 1,990 MHz with 100 kHz steps. The VDS-6600 uses a reference of 1 MHz into the phase detector while still providing the required 100 kHz steps. The programmable fractionality of 10 improves the close-in phase noise by almost 20 dB over a traditional single loop PLL.

For more information on the ALL™ architecture, consult the factory for a listing of the published articles on this subject.

2. PERFORMANCE/SPECIFICATIONS

Frequency

Range 1,850 MHz to 1,990 MHz

Step Size 100 kHz

Control 19-bit parallel

Main Output

Level +10 dBm into 50Ω

Flatness ±1 dB

Spectral Purity

Harmonics <-20 dBc

Spurious <-60 dBc

Phase Noise, typical

1 kHz offset <-80 dBc/Hz

10 kHz offset <-90 dBc/Hz

100 kHz offset <-105 dBc/Hz

Frequency Ref External 10 MHz @ 0 dBm ±3 dB

Ref Output (J3) 10 MHz @ >+10 dBm

Lock Indicator “0” for Out-of-Lock (TTL compatible) plus LED

Connectors

RF Output (J5) SMA female

RF Output (J4) SMA female — not used

Ref Input (J2) SMA female

Ref Output (J3) SMA female

Freq Control/Pwr (J1) 25-pin male subminiature “D”



VDS-6600-1436 OPERATING INSTRUCTIONS

2. PERFORMANCE/SPECIFICATIONS (continued)

Power Supply+5V @ 450 mA; +15V @ 150 mA

Environmental

- Operating Temp.....0°C to +50°C
- Storage Temp.....-20°C to +70°C
- Dimensions.....4.5" x 4.74" x 1.125"
- Weight<1 lbs, net; 4 lbs, shipping

3. MECHANICAL CONFIGURATION

The VDS-6600 is manufactured on a single printed circuit board with a 25-pin (male) subminiature “D” connector located on one 4.74” edge. Both the Ext Ref Input and the RF output are located on the same 4.74” edge of the board as the 25-pin subminiature “D” connector that is used to apply frequency control and power. An out-of-lock indicator LED is located between the 25-pin connector and the External REF Input. The Main RF Output is located on the opposite 4.74” edge and a second channel at half of the main output is also available.

Function	Connector	Mating Connector
Frequency Control (J1)	25-pin Submini “D”	Amphenol 117DB-25P or equivalent
RF Out (J4)	SMA female	SMA male
RF Out (J5)	SMA female	SMA male
Ext Ref In (J2)	SMA female	SMA male
Ext Ref Out (J3)	SMA female	SMA male

4. PIN ASSIGNMENTS

Both parallel and serial control pin assignments (S_Data, S_CLK, & S_LE) are shown in the following table:

Pin No.	Description	Pin No.	Description	Pin No.	Description
1	NC	9	M4	18	N5
2	N0 / S_Data	10	K1	19	N7
3	+24V	11	K3	20	M1
4	N2	12	K5	21	M3
5	N4 / S_CLK	13	STROBE	22	K0
6	N6 / S_LE	14	LCK1	23	K2
7	M0	15	N1	24	K4
8	M2	16	+5V	25	GND
		17	N3		

Frequency Control Programming Lines (J1)



5. REFERENCE FREQUENCY

The VDS-6600-1436 board has been designed to operate from an external REF of 10 MHz with 0 dBm ±3 dB level.

6. REFERENCE SELECTION

With parallel control, several parameters are hardwired within the synthesizer. The “R”, “F” and “P” registers are set at the factory, as is the Modulus Polarity bit (MP) and others as described below.

R Register	This register is a programmable number that selects the actual frequency used by the phase detector. For the VDS-6600-1436, this number has been hardwired to 10 to provide a 1 MHz phase detector frequency.
F Register	This register selects the fractionality used by the SEI-1618. For the VDS-6600-1436, the Fractionality has been hardwired to 10 to generate 100 kHz steps (1 MHz ÷ 10).
P Register	This register stores the value of the lower number for the dual modulus. For the optional parallel control, this register is hardwired internally to 32 for the VDS-6600-1436.

7. OPERATION — parallel control

With the optional Parallel-to-Serial converter, the user can program the synthesizer with parallel control. An FPGA device is included which converts the parallel data provided by the customer into the serial data needed by the SEI-1618PG fractional PLL chip. All signal levels are TTL compatible.

7.1 Frequency Control

Due to the use of a ÷32/33 dual modulus, the minimum divide ratio is 992 (P • [P-1]). The reference into the phase detector (determined by the reference divider) determines the division ratio. With the 1850 MHz minimum frequency of the VDS-6600-1436 and the use of the ÷32/33, the maximum useable reference frequency becomes approximately 1.8 MHz. This does not mean that a higher frequency could not be used in this scenario but it does mean that you would not be able to cover the entire range of 1,850-1,990 MHz with 100 kHz steps. With a larger reference frequency, there would be some frequencies that simply could not be programmed.



8. GLOSSARY OF TERMS

The following section describes the different terms used in the ALL™ architecture (Main Loop). The range of values valid for each parameter and any suggested configuration are given where applicable.

8.1 Reference Frequency

The external reference frequency is supplied to the female SMA connector (J2). This frequency determines the values used in the N, M, and K registers described later. The nominal value is 10 MHz although other values are possible.

8.2 Reference Divider (R)

The Reference Divider, R register, determines the actual reference into the digital phase detector. Permissible values for the R register are 2 to 32 (5 binary bits). Although the actual number loaded into the register is one less than the desired number. The R register is hardwired to 10 for the VDS-6600-1436.

8.3 Fractionality (F)

The fractionality is the heart of the ALL™ and is what improves the close-in phase noise performance over the performance of a single PLL. Permissible values for the F register are 2 to 64 (6 binary bits) although the actual number loaded into the register is one less than the desired number. In the VDS-6600-1436, the fractionality is hardwired to 10.

8.4 Frequency Resolution (step size)

The frequency resolution or step size of the main loop is determined by a combination of the reference frequency, the reference divider (R register), and the selected fractionality, F register. In the VDS-6600-1436, the reference into the phase detector is 1 MHz so the R register becomes 10. With a fractionality of 10, the frequency step size is therefore calculated as follows:

$$F_{\text{step}} = f_{\text{CLOCK}} \div R \div F \quad (\text{Eq 1})$$

Note that the actual frequency resolution also includes any fixed prescalers ($\div D$) used in the circuit (to bring the output frequency into a range that can be handled by the counters). For the VDS-6600-1436, no additional divider is required to reduce the frequency into the dual modulus prescaler ($\div 32/33$). The formula for the step size is therefore modified as follows:

$$F_{\text{step}} = f_{\text{CLOCK}} \div R \div F \cdot D \quad (\text{Eq 2})$$



$$F_{\text{step}} = 10 \text{ MHz} \div 10 \div 10 = 100 \text{ kHz}$$

8.5 Main Divider (N)

The N register determines the number of clocks that the dual modulus will divide by MOD1 (smaller of the two choices for the dual modulus — 32 for the VDS-6600-1436). Permissible values for the N register are 0 to 255 (8 binary bits) but are limited to 57-62 for the VDS-6600-1436.

Note that the value of the N register **MUST BE GREATER** than the value of the M register.

8.6 Modulus Divider (M)

The M register determines the number of clocks that the dual modulus will divide by MOD2 (larger of the two choices for the dual modulus — 33 for the VDS-6600-1436). Permissible values for the M register are 0 to P-1 where P is the lower number of the dual modulus used. (5 binary bits, maximum = 31).

8.7 Fractional Divider (K)

The K register controls the smallest steps in the synthesizer by allowing additional divisions by MOD2 (larger of the two choices for the dual modulus — 33 for the VDS-6600-1436) within each period determined by the phase detector reference (1 MHz in this case). Permissible values for the K register are 0 to F-1 where F is the fractionality chosen (6 binary bits, maximum = 63).

8.8 Phase Polarity (PP)

This one bit allows for the electrical switching of the \emptyset_R and \emptyset_V outputs from the phase detector. The outputs of the phase detector (pins 3 and 5) on the SEI-1618PG (U4) will switch with the toggling of this bit. Set this bit to 0.

8.9 Modulus Polarity (MP)

This one bit allows for the electrical switching (polarity) of the modulus control line (pin 10 of the SEI-1618PG) to provide compatibility with all known dual modulus devices whether they are positive or negative triggered. For most dual modulus prescalers, the lower divide number (P) is selected when the modulus control line is HIGH. The Modulus Polarity bit (MP) should be set to LOW (“0”) for these units. Use MP = 1 if the lower divide number (P) is active when the modulus control line (pin 10 on the SEI-1618PG) is LOW.



9. FREQUENCY CALCULATION

These terms, N, M, & K are calculated as:

Total Division Ratio, $T = (N - P) \cdot P + M \cdot (P + 1) = F_{out} \div F_{ref}$

where F_{ref} is the phase detector frequency and F_{out} is the Main output.

And the parameters can be calculated as follows:

- 1.) $N = INT [T \div P]$
- 2.) $M = INT [\{ (T \div P) - N \} \cdot P]$
- 3.) $K = [\{ (T \div P) - N \} \cdot P - M] \cdot P$

10. PROGRAMMING EXAMPLES

Several examples will be presented to assist the user in determining the values needed for each register. Note that the F Register is always set to 10 and the R Register is always set to 10 and have been omitted from the table.

DESIRED FREQUENCY	REGISTERS		
	N	M	K
1,8500.00 MHz	57	26	0
1,850.100 MHz	57	26	1
1,899.900 MHz	59	11	9
1,900.000 MHz	59	12	0
1,989.100 MHz	62	5	1
1,990.000 MHz	62	6	0

11. ALARM (Lock Indicator)

Pin 14 of the 25-pin connector contains the lock indicator control line. This line provides access to the status of the PLL loop. The signal is a TTL level voltage. The following table contains the logic state for Lock/Out-of-Lock indication. In addition, there is a red LED next to the 25-pin connector that will illuminate when an out-of-lock condition is present (either there is no external reference, an illegal frequency has been programmed, or the loop has broken lock and may need to be returned for repair).

INDICATION	LOCK LINE LEVEL
PLL Locked	TTL HIGH
PLL Out-of-Lock	TTL LOW

Lock Indicator Logic



12. WARRANTY

All Meret products are warranted against defects in material and workmanship for a period of one year after initial shipment. Meret will repair or replace any circuit or component that is found to be defective during this period if in Meret's sole opinion the product is deemed defective.

Any modifications or options performed by Meret during the initial one year period shall be included under the initial warranty, and such secondary warranties shall terminate one year after the initial shipment. Shipment of the product to Meret (San Diego, CA) shall be made prepaid and shall not be made without prior authorization by Meret.

This warranty is voided if the product is abused or if unauthorized modifications are made by the user.

This warranty is in lieu of all other warranties, expressed or implied, and no person is authorized to represent or assume for Meret any liability in connection with the sales of our products other than stated within this warranty.

Serial Number

QC by _____ Date: _____