

# OPERATING INSTRUCTIONS

## VDS-9201-1214 Frequency Synthesizer

### 1. PRODUCT DESCRIPTION

The VDS-9201-1214 is a remote controlled serial frequency synthesizer designed to operate in the band from 672 MHz to 1008 MHz with programmable frequency resolution and good spectral purity. This product uses a single power supply (+15V) at low power to provide a versatile signal source for many applications.

### 2. PERFORMANCE/SPECIFICATIONS

#### Frequency

Range .....	672 MHz to 1008 MHz
Resolution .....	25 kHz
Control .....	Serial Binary Positive-true TTL logic
Switching Speed .....	100 msec, maximum

#### Main Output

Level .....	+3 dBm $\pm$ 2 dB into 50_
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#### Spectral Purity

Harmonics .....	<-20 dBc
Spurious .....	<-60 dBc
Phase Noise	
100 Hz offset.....	<-55 dBc/Hz
1 kHz offset.....	<-60 dBc/Hz
10 kHz offset.....	<-85 dBc/Hz
100 kHz offset.....	<-115 dBc/Hz

#### Frequency Ref.....

Internal Accuracy.....	$\pm$ 1 ppm (optional)
External Level.....	0 dBm $\pm$ 3 dB

#### Lock Indicator .....

#### Connectors

RF Out.....	SMA female (J2)
Freq Control.....	14-pin IDC dual row header (JP1)

#### Power Supply .....

#### Environmental

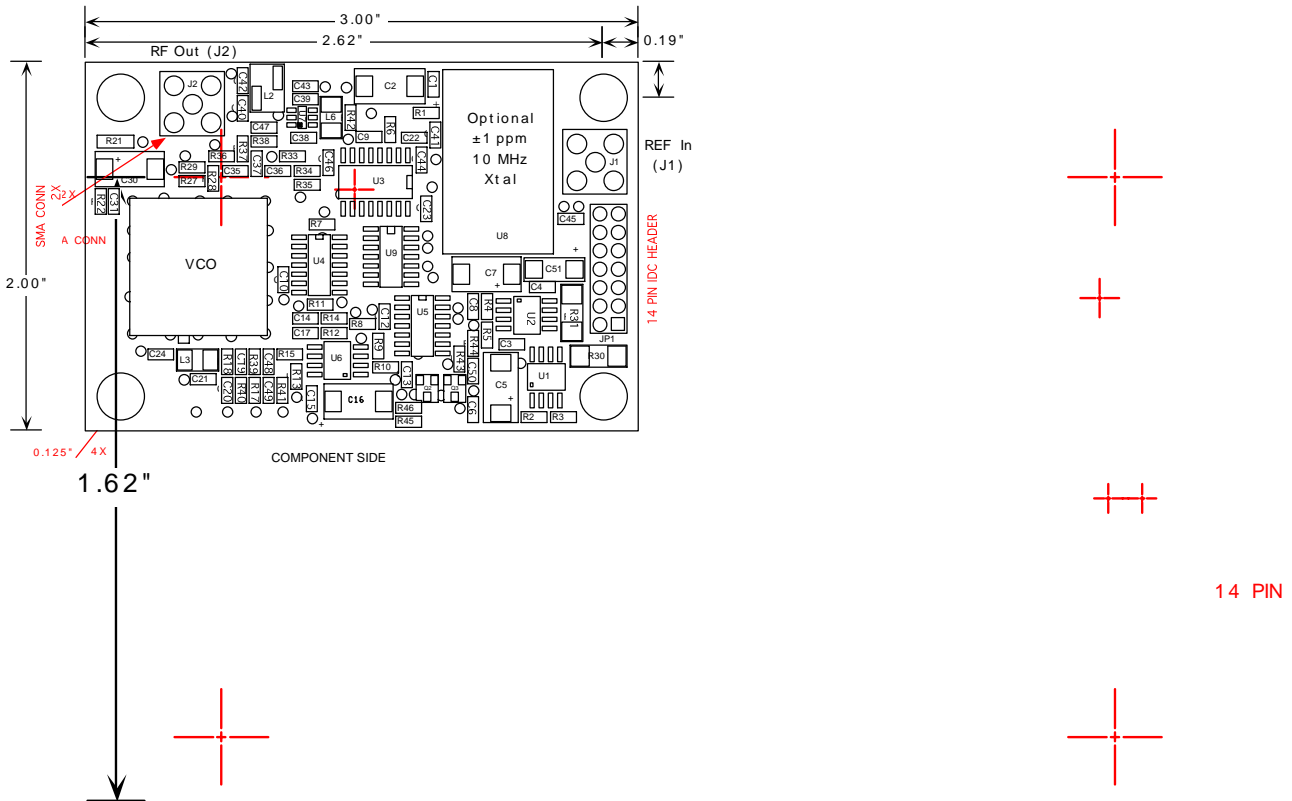
Operating Temp .....	0°C to +50°C
Storage Temp .....	-20°C to +70°C
Dimensions .....	2" x 3" x 0.4" (pcb)
Weight.....	<1 lbs, net; 3 lbs, shipping



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## 3. MECHANICAL CONFIGURATION

The VDS-9000 synthesizer family is manufactured in a single printed circuit board with an on-board  $\pm 1$  ppm crystal (if ordered). The output RF signal (J2) is accessed through an SMA female connector mounted to the board. Frequency Control is accomplished through a 14-pin IDC header (JP1) located next to the output RF connector.



## 4. POWER SUPPLY CONNECTIONS

Power is supplied to the 14-pin connector as follows:

Power Supply	Pin Number
+15V	1 & 2
Ground	3



**5. PIN ASSIGNMENTS**

The three signals, Data Clock, Load Enable and Data are accessed on the 14-pin IDC connector along with the power supply and ground according to the following table:

Pin No.	Description	Pin No.	Description
1	___ V dc ( $V_{cc}$ )	8	CLOCK
2	___ V dc ( $V_{cc}$ )	9	GND
3	GND	10	DATA
4	Lock Detector	11	GND
5	GND	12	LATCH
6	GND	13	GND
7	GND	14	GND

Frequency Control Programming Lines (JP1)

**6. REFERENCE FREQUENCY**

The VDS-9201-1214 has been designed to operate from an internal 10 MHz reference with better than  $\pm 1$  ppm accuracy/stability (if ordered). A 10 MHz output monitor is available on the J1 SMA (not installed) at greater than -15 dBm if the internal 10 MHz reference option was installed.

**7. FREQUENCY CONTROL (per MB1501 logic control)**

All control lines should be driven with standard TTL levels ("0" = 0V to 0.4V for "LOW" and "1" = 2.4V to 5V for "HIGH".) Registration of the signal occurs in the synthesizer once data has been clocked into the synthesizer.

The control follows a serial loading sequence with two words determining the output frequency (reference divider and output divide ratio). The first 14-bit word determines the reference frequency or step size ( $R_{14} R_{13} \dots R_2 R_1$ ) while the second word determines the PROGRAMMABLE DIVIDERS or output frequency ( $P_{18} P_{17} P_{16} \dots P_2 P_1$ ).



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The actual programming involves seven steps as follows:

x(1) Load a TTL “1” (determines if the  $\div 128/129$  or  $\div 64/65$  is used). 1 \_  $\div 64/65$ .

x(2) Calculate Reference Divider Word (**R<sub>14</sub> R<sub>13</sub> ... R<sub>2</sub> R<sub>1</sub>**):

Since the synthesizer uses a 10 MHz internal crystal (see section 6), this number becomes 100 for a 100 kHz step. Convert these numbers to binary:

$$(100 \_ 00 \mid 0000 \mid 0110 \mid 0100)$$

Load reference divider (14 bits).

x(3) Load a TTL “1”

x(4) Pull the LOAD ENABLE bit “HIGH” to assert it and then release the line.

x(5) Calculate the PROGRAMMABLE DIVIDER word (**P<sub>18</sub> P<sub>17</sub> P<sub>16</sub> ... P<sub>2</sub> P<sub>1</sub>**):

a. Divide the desired frequency by the desired step size.

b. Divide this number by 64 and take the integer portion as the value for the 11 bits of the programmable divider (P<sub>8</sub> .. P<sub>18</sub>). The remainder becomes the value for the swallow counter (P<sub>1</sub> .. P<sub>7</sub>). The ranges for the these two words are 16 to 2047 for the programmable divider (P<sub>8</sub> .. P<sub>18</sub>) and 0 to 127 for the swallow counter (P<sub>1</sub> .. P<sub>7</sub>).

x(6) Convert both values to binary and then load in the 11 bits of the programmable divider followed by the swallow counter word (7 bits).

x(7) Load a TTL “0”

x(8) Clock the data into the synthesizer by asserting the LOAD Enable bit and then releasing it.

**Note that one bit of data is clocked into the registers on the rising edge of the data clock and that data is loaded starting with the MSB of each word.**

Upon the completion of all three words plus the control bits (steps 1, 3, & 4), the LOAD Enable bit clocks the data into the synthesizer on the rising edge.

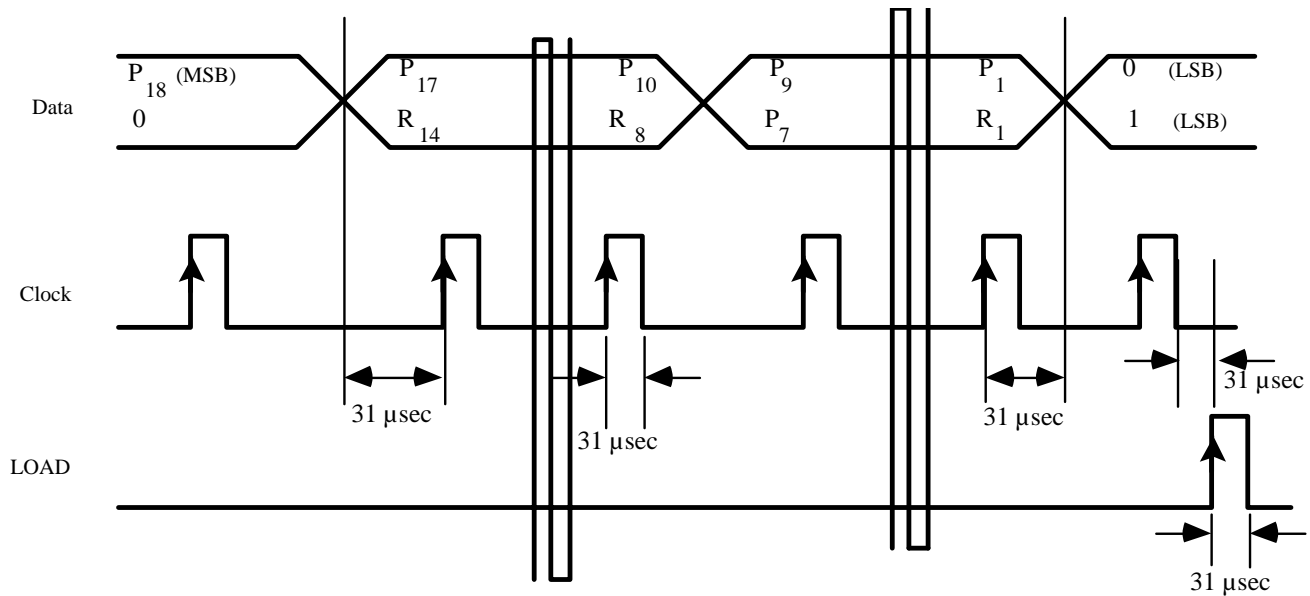


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In summary, the desired frequency is programmed according to the following formula:

$$\text{Programmable Divider (N}_T\text{)} = f(\text{Desired Frequency (MHz), Step Size (MHz)}) = (64 \cdot N + A)$$

where  $N = \text{Integer (N}_T \div 64)$  and  $\text{Swallow Counter (A)} = N_T - N \cdot 64$



### 8. ALARM (Lock Indicator)

Pin 4 of the 14-pin IDC connector contains the lock indicator control line. This line provides access to the status of the PLL loop. The signal is a TTL level voltage according to the values in the following table:

INDICATION	LOCK LINE LEVEL
PLL Locked	TTL HIGH
PLL Out-of-Lock	TTL LOW

Lock Indicator Logic



## 9. PROGRAMMING EXAMPLE

One programming example will be presented to assist the user in determining the pin configurations for a desired frequency.

x(1) An output frequency of 923.4 MHz is desired.

In order to set a frequency of 923.4 MHz, the following words should be used:

The Reference Frequency divider becomes 100 ( $10 \text{ MHz} \div 100 \text{ kHz}$ ). Therefore the reference frequency word becomes:

00 | 0000 | 0110 | 0100<sub>2</sub> or 0064<sub>H</sub>

The programmable divider becomes 9234 ( $923.4 \text{ MHz} \div 100 \text{ kHz}$ ). Divide this by 64 and the integer portion ( $144_{10}$  or  $090_{H}$ ) becomes the 11-bit word and the remainder ( $18_{10}$  or  $12_{H}$ ) becomes the 7-bit word as follows:

000 | 1001 | 0000<sub>2</sub> ( $090_{H}$ ) and 001 | 0010<sub>2</sub> ( $12_{H}$ ) or as one word:

00 | 0100 | 0100 | 00001 | 0010<sub>2</sub> ( $04412_{H}$ )

Remember that the MSB must be programmed first.



**10. WARRANTY**

All Meret products are warranted against defects in material and workmanship for a period of one year after initial shipment. Meret will repair or replace any circuit or component that is found to be defective during this period if in Meret's sole opinion the product is deemed defective.

Any modifications or options performed by Meret during the initial one year period shall be included under the initial warranty, and such secondary warranties shall terminate one year after the initial shipment. Shipment of the product to Meret (San Diego, CA) shall be made prepaid and shall not be made without prior authorization by Meret.

This warranty is voided if the product is abused or if unauthorized modifications are made by the user.

This warranty is in lieu of all other warranties, expressed or implied, and no person is authorized to represent or assume for Meret any liability in connection with the sales of our products other than stated within this warranty.

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Serial Number

QC by \_\_\_\_\_ Date: \_\_\_\_\_

