OPERATING INSTRUCTIONS

DCP-1 Digital Chirp Processor System
DCP-1A Digital Chirp Processor Module

1. PRODUCT DESCRIPTION

The DCP-1 Direct Digital Chirp Synthesizer is composed of the DCP-1A Digital Chirp Synthesizer module plus additional support circuitry and housed in a 5.25” rack mountable chassis. It uses GaAs technology to operate from 1 to 230 MHz with <30 Hz frequency resolution. A proprietary and custom GaAs gate array is used to achieve the combination of wide frequency bandwidth, fine resolution, and ultra fast switching speed that is necessary for low granularity chirps. Phase control (up to 12-bits) are provided to allow for compensation of test circuits as well as precise phase modulation control.

A 500 MHz clock oscillator locked to an internal or external 10 MHz reference is supplied in a separate module as a standard feature to provide the necessary clock frequency for the chirp processor.

In addition, some interface logic is provided in a separate module to buffer the 24 data lines and 9 control lines used in the DCP-1A and a single +28V power supply with an optional AC voltage (either 115V or 230 V) is provided.

2. OPTIONS AND CONFIGURATIONS

DCP-1A — Single 5” x 7.08” x 1.125” module that requires an external 500 MHz reference. It is clocked at 500 MHz so an anti-aliasing filter with a low pass cutoff frequency of 230 MHz is required by the user.

DCP-1A/LPF — Single 5” x 7.08” x 1.125” module containing an internal 230 MHz low pass filter and gain equalization. Note that filter is not optimized for linear phase.
DCP-1A/Q—2-channel version of the above, 1 with filter, one without, or both without.

DCP-1A/LPF-1283 — same as DCP-1A/LPF except that MAIN Select, AUX Select, ROM Reset, CLK Reset and ADD Zero control lines are ECL compatible

DCP-500A — 500 MHz DRO reference generator for use as the DDS clock with the DCP-1A.

DCP-230LPF — 230 MHz low pass filter module for use with the DCP-1A. Filter is not optimized for a linear phase response.

DCP-1/28 — 5.25” rack mountable chassis that contains the DCP-1A, DCP-500A, DCP-230LPF*, power supply for operation from +28V, and TTL line driver module.

DCP-1/VAC — Same as the DCP-1/28 except that it requires 115Vac or 230Vac mains.

* can be included within the DCP-1A/LPF.

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3. PERFORMANCE/SPECIFICATIONS: DCP-1A

Output Frequency
Range (DCP-1A) ....1 MHz to 250 MHz (w/o LPF)
Range (DCP-1A/LPF)......1 MHz to 230 MHz (w/ LPF)
Resolution.......................<30 Hz (Approximately 29.80… Hz)
Control............................24 parallel BINARY TTL bits (pos-true logic) with STROBE
Main Output (with LPF and gain equalization)
Level ....-5 dBm into 50Ω (1 MHz to 230 MHz)
Accuracy/Flatness...........±2 dB
Phase Control......................12 parallel TTL Binary bits (pos-true logic)
Spectral Purity
Harmonics.......................-35 dBc
Spurious (typical)............-50 dBc (@<100 MHz)
-45 dBc (@ >200 MHz)
Phase Noise @ 101 MHz.<-95 dBc/Hz @ 100 Hz offset
<-95 dBc/Hz @ 1 kHz offset
<-115 dBc/Hz @ 10 kHz offset
<-130 dBc/Hz @ 100 kHz offset
Clock Frequency.................500 MHz
Level ....+5 dBm ± 2 dB
Reference Frequency (if optional REF GEN module is supplied)
External...........................10.0 MHz @ 2 dBm ± 2 dB into 50Ω
or
Internal............................10.0 MHz @ ±1 ppm accuracy
Frequency Switching
Switching Speed ....<2 **NANO**seconds in the chirp mode
<50 nsec in manual hopped CW mode
Characteristic...................Phase Continuous (Linear FM mode only)
Connectors
RF Sine Output................SMA Female (J1)
DDS Clock Ref Input.......SMA Female (J3) - 500 MHz
Frequency Control ....50-pin mini D-connector (P2)
Power...............................9-pin mini D-connector (P1)
Stop Frequency................15-pin mini D-connector (P3)
Environmental
Operating Temp...............0°C to +50°C
Storage Temp...................-20°C to +70°C
Power Supply......................-5.2V @ 2.5A; +5V @ 150 mA; -12V @ 125 mA; -2V @ 500 mA
Dimensions..........................5"(W) x 7.08"(D) x 1.125"(H);
Weight.................................2 lb (0.9 kg), net; 3 lbs (1.4 kg), shipping

3.1 PERFORMANCE/SPECIFICATIONS: DCP-1

Output Frequency	
Range	1 MHz to 230 MHz (contains LPF)
Resolution	<30 Hz (Approximately 29.80… Hz)
Control	24 parallel BINARY TTL bits (pos-true logic) with STROBE
Phase Control	12 parallel TTL binary bits (positive true logic)
Main Output	
Level	-5 dBm into 50Ω
Accuracy/Flatness	±2 dB
Auxiliary Output #2 — Optional	
Frequency	125.0 MHz
Level	>0 dBm into 50Ω
Spectral Purity	
Harmonics	-35 dBc
Spurious (typical)	-50 dBc (@<100 MHz)
	-45 dBc (@ >200 MHz)
Phase Noise @ 101 MHz	<-95 dBc/Hz @ 100 Hz offset
	<-95 dBc/Hz @ 1 kHz offset
	<-115 dBc/Hz @ 10 kHz offset
	<-130 dBc/Hz @ 100 kHz offset
Clock Frequency	500 MHz, internally phase locked to Reference Frequency
Reference Frequency	
External	10.0 MHz @ 2 dBm ± 2 dB into 50Ω , **OR**
Internal	10.0 MHz @ ±1 ppm accuracy
Frequency Switching	
Switching Speed	<2 **NANO**seconds in the chirp mode
	<50 nsec in manual hopped CW mode
Characteristic	Phase Continuous (Linear FM mode only)
Connectors	
RF Sine Output	SMA Female (MAIN OUT)
Stop Frequency	15-pin subminiature "D" connector (STOP FREQ)
DDS Clock (500 MHz)	SMA Female (CLOCK OUT)
DDS Clock ÷4 (125 MHz)	SMA Female (AUX2) — optional
Ref Input	SMA Female (10 MHz IN)
Ref Output	SMA Female (10 MHz OUT)
Frequency Control	50-pin subminiature D-connector (P2)
Power	either Banana Jacks for DCP-1/28 or
	optional AC receptacle (DCP-1/115 or DCP-1/230)
Environmental	
Operating Temp	0°C to +50°C
Storage Temp	0°C to +70°C
Power Supply	+28V @ 3A (DCP-1/28); 115 Vac @ 60 Watts (DCP-1/115)
Dimensions	5.25"(H) x 16"(D) x 17"(W);
Weight	14 lb (6.4 kg),net; 18 lbs (8.2 kg), shipping

4. MECHANICAL CONFIGURATION

DCP-1A

The DCP-1A is built according to best commercial practice. The chirp processor itself is housed in a 5” x 7.08” x 1.125” metal module with a 50-pin subminiature “D” connector on one 5” x 1.125” surface. A 9-pin subminiature “D” connector, used for connecting the DCP-1A to DC power, is located on the same face.

The opposite 5” x 1.125” face contains the RF connectors (SMA Female) such as DDS Clock REF Input and RF Output and a 15-pin subminiature “D” connector for the STOP Frequency. Refer to the section on Signal Connections for a listing of the possible connections.

IMPORTANT NOTE

> The DCP-1A module containing the GaAs circuitry consumes approximately 15 watts of power. Heat sinks are employed to aid in heat dissipation but it is important that air be passed over the module in order to further reduce the heat build up.

DCP-1

The DCP-1 chassis contains the DCP-1A chirp module and a DCP-500A reference generator module mounted horizontally near the center of the chassis (units sold before 1/1/94 contained the DCP-500 SAW based reference generator). A fan is mounted on the rear panel and blows outside air over these modules. A separate chamber houses the power supply conditioning module (whether it is derived from 115/230 Vac or +28V). All of the signals are located on the rear panel except for the LED lock indicator for the 500 MHz generator which is located on the front panel with the power switch and mains power indicator.

4. INSTALLATION

4.1 DCP-1A ALONE

The DCP-1A requires an external 500 MHz clock at +5 dBm ±2 dB. As this is the master clock for the synthesizer, its spectral purity will determine the performance of the synthesizer. The phase noise at the output is within 3 dB of the phase noise of the reference except that the noise floor of the synthesizer is limited to -145 dBc/Hz. No low pass filter is included within the DCP-1A (can be optionally ordered as a separate module or it can be included at no additional charge inside the module — specify DCP-1A/LPF instead of the DCP-1A).

4.2 WITH THE OPTIONAL REF GEN MODULE (use with DCP-500A only)

Internal / External REF Selection

The DCP-1 is configured such that the user when ordering can choose between an internal or external 10 MHz reference. The user manually selects the internal reference or external reference with the **toggle switch** on the rear panel of the DCP-1. When an external reference is selected, a red LED near the switch will illuminate.

If the DCP-500A reference generator module is ordered with the DCP-1A, the external reference is applied to the external 10 MHz input SMA (J1) on the reference generator module. The internal reference is selected **by shorting together Pins 2 & 4** on the 9-pin subminiature D-connector (P1). If these two pins are left unconnected, the internal 10 MHz crystal is disabled and the 500 MHz DRO resonator will free run.

CAUTION

Do **NOT** ground pin 2 as this line contains the +12V required to power up the 10 MHz (when shorted to pin 4).

For details on the older, discontinued DCP-500 (SAW Resonator based), please consult the factory directly.

4.3 FREQUENCY CONNECTION

Caution must be taken when wiring up a mating connector. Different style connectors use different conventions in the numbering scheme (either left-to-right or up-and-down). Refer to sections 12.2 and 12.3 for the pin assignments on the DCP-1 Chassis and DCP-1A module respectively.

Note that a mating cable built for the DCP-1 chassis will operate correctly with the DCP-1A module. The only reason for a different numbering scheme on each connector is the different convention used by the connector manufacturer for each style connector (i.e., bulkhead ribbon connector used on the DCP-1 chassis and right angle PC mount on the DCP-1A module).

WARNING

Due to the static sensitivity of some of the synthesizer components, it is important that all the necessary precautions are taken to prevent static damage including but not limited to the use of ground straps and proper grounding techniques. Ground connections must be made first before connecting the frequency control mating connector to discharge any built-up static charge.

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5. POWER SUPPLY CONNECTIONS AND REQUIREMENTS (DCP-1A)

The +5V, -5.2V, -2V and -12V DC power supplies are connected to the 9-pin subminiature “D” connector (P1) as follows:

POWER SUPPLY	CURRENT	PIN #
+5V	150 mA	1 & 2
-2V	500 mA	6
-5.2V	2.50 A	4 & 5
-12V	125 mA	3
GND	----	7 & 8

5.1 POWER SUPPLY CONNECTIONS AND REQUIREMENTS: Reference Generator

The +5V and ±12V DC power supplies are connected to the 9-pin subminiature “D” connector (P1) as follows:

DCP-500

POWER SUPPLY	CURRENT	PIN #
+5V	200 mA	1
+12V	150 mA	9
-12V	10 mA	3
GND	----	7 & 8

DCP-500A

POWER SUPPLY	CURRENT	PIN #
+5V	250 mA	1
+12V	100 mA	9
GND	----	7, 8

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6. SIGNAL INPUT/OUTPUT CONNECTION

Several signals may be connected to the DCP-1A. The signals may be accessed according to the following table:

Output Signal	Female SMA Number
RF Sine Output	J1

Input Signal	Female SMA Number
500 MHz Reference Input	J3

The connectors on the Clock Reference module are listed in the following table:

Signal	Level	Connector	
		Label	Type
Power Supply	N/A	P1	9-pin submini “D”
10 MHz Input	0 dBm ± 2 dB	J1	female SMA
10 MHz Output	>-15 dBm	J2	female SMA
500 MHz Output	>+10 dBm	J3	female SMA
Not Used	N/A	J4	female SMA
500 MHz Output	>+5 dBm	J5	female SMA

Table 5.2

6.1 SIGNAL INPUT/OUTPUT CONNECTION (DCP-1)

Several signals may be connected to the DCP-1. The signals may be accessed according to the following table:

Output Signal	Female SMA Designation
RF Sine Output	MAIN OUT
Ref Output	10 MHz OUT
500 MHz Clock Output	CLOCK OUT
DDS Clock ÷4 — Optional	AUX2

Input Signal	Female SMA Designation
Reference Input	10 MHz IN
Stop Frequency Input	STOP FREQ (15-pin Subminiature “D”)

IMPORTANT NOTE

The 10 MHz output is not buffered so this connection must not be shorted or grounded. Doing so will result in a frequency shift of the output signal, since the output will not be locked to the 10 MHz reference.

7. SIGNAL DESCRIPTION

MAIN Start Register (TTL) — 24-bit word that stores the starting frequency for a chirp (sweep).

AUX Start Register (TTL) — 24-bit word that stores the starting frequency for a second chirp (sweep).

Increment Register or “Chirp Rate” (TTL) — 24-bit word that stores the step size that will be added to either the MAIN or AUX Start register (depending on which Select is used) every 2 nsec. **A negative slope (chirp rate) is possible by programming a 2’s complement of the desired chirp rate.**

Mode Select (TTL) — 2-bit word that multiplexes the 24-bit data buss between the MAIN Start register, AUX Start register and Increment register.

Strobe (TTL) — 1-bit, level triggered, for synchronizing loading data into each of the registers.

MAIN Select (TTL) — 1-bit that activates and selects the MAIN Start Register as the register for use in the sweep. Use to control the chirp if the MAIN Start Register contains the desired start frequency. Optionally available as ECL compatible.

AUX Select (TTL) — 1-bit that activates and selects the AUX Start Register as the register for use in the sweep. Use to control the chirp if the AUX Start Register contains the desired start frequency. Optionally available as ECL compatible.

ROM Reset (TTL) — 1-bit that turns off the output by disabling the ROM so phase information is maintained (i.e., accumulators continue to run). Optionally available as ECL compatible.

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MSTR Reset ($\overline{TTL}$) — 1-bit that is used to initialize the chirp and can be used to force the output to zero. Active LOW.

CLK Reset ($\overline{TTL}$) — 1-bit that can be used to freeze the chirp at a given point. Releasing this line causes the chirp to continue from last output frequency. Active LOW. Optionally available as ECL compatible.

ADD Zero ($\overline{TTL}$) — 1-bit that disables the 12-bit phase modulation capability. Active LOW (when asserted no phase shift is possible). Optionally available as ECL compatible.

STOP Frequency (TTL) — 8 Most significant bits from frequency accumulator to allow more precise control of the chirp width.

8. THEORY OF OPERATION

The DCP-1/DCP-1A is composed of three GaAs devices. The architecture (phase accumulator, ROM and DAC) is similar to the more traditional Direct Digital Synthesizers (DDS) with one additional feature. The accumulator is actually composed of a dual accumulator (chirp chip). There is a standard 24-bit phase accumulator to drive the 14-bit x 12 ROM (sine look up table) but another 24-bit FREQUENCY accumulator has been added in front of the phase accumulator to add linear sweep capability. The advantage of combining two accumulators in one package is speed. The update rate for the synthesizer in the sweep mode is every clock cycle — 2 nsec!

The output of the chirp chip is equivalent to that of a double digital integrator and produces a quadratic phase function. The desired chirp rate can be calculated from the following equation where W is the normalized increment (i.e., step size ÷ smallest available step, 29.802 Hz) and F_{clk} is the DDS clock (in MHz):

$$\textbf{Chirp Rate (kHz/}\mu\textbf{sec)} = \frac{F_{clk}^2 \cdot W}{2^{24}} * 1000 \qquad (1)$$

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In order to calculate the closest step size from a desired chirp rate, use the following formula:

$$\textbf{Step size (kHz)} = \mathbf{W} \bullet \frac{\mathbf{F_{clk}}}{\mathbf{2^{24}}} = \frac{\text{Chirp Rate (kHz/µsec)} \bullet 2^{24}}{F_{clk}^{2}} \bullet \frac{F_{clk}}{2^{24}} =$$

$$= \frac{\textbf{Chirp Rate (kHz/µsec)}}{\mathbf{F_{clk}}\ \textbf{(MHz)}} \qquad \textbf{(2)}$$

Where the minimum chirp rate (W = 1) is 14.9 kHz/µsec and the minimum step size is 29.8 Hz (for a 500 MHz DDS clock).

Example 1:
Suppose that a chirp covering 40 MHz in 5 µsec is desired. The chirp rate becomes:

$$\text{Chirp Rate} = \frac{40\ \text{MHz}}{5\ \text{µsec}} = 8\ \text{MHz/µsec} = 8000\ \text{kHz/µsec}$$

The required step size (kHz) is:

$$= \frac{8000}{500} = 16$$

The closest step size is calculated as:

$$\textbf{Programmed Step Size} = \textbf{INT}\left(\frac{\textbf{Desired Step size}}{\mathbf{F_{clk}} \div \mathbf{2^{24}}} + \mathbf{0.5}\right) \bullet \frac{\mathbf{F_{clk}}}{\mathbf{2^{24}}} \qquad \textbf{(3)}$$

For this example, the programmed step size becomes 16.003 kHz and the actual chirp rate, Equation (1), becomes 8,002 kHz/µsec rather than 8,000 kHz/µsec.

Example 2:
Suppose that a chirp covering 120 MHz in 500 nsec is desired. The chirp rate becomes:

$$\text{Chirp Rate} = \frac{120\ \text{MHz}}{500\ \text{nsec}} = 0.24\ \text{MHz/nsec} = 240{,}000\ \text{kHz/µsec}$$

The required step size (kHz) is:

$$= \frac{240000}{500} = 480$$

For this example, the programmed step size becomes 479.996 kHz and the actual chirp rate, Equation (1), becomes 239,998 kHz/µsec rather than 240,000 kHz/µsec.

Example 3:
Suppose that a chirp covering 25 MHz in 5 msec is desired. The chirp rate becomes:

$$\text{Chirp Rate} = \frac{25\ \text{MHz}}{5\ \text{msec}} \qquad = 5\ \text{MHz/msec} = 5\ \text{kHz/}\mu\text{sec}$$

Since the required chirp rate is less than the minimum of 14.9 kHz/µsec, this chirp is not possible with a 500 MHz clock. With a chirp bandwidth of only 25 MHz, it would be possible to reduce the DDS clock and thereby slow down the minimum chirp rate.

If F_{clk} were reduced to 150 MHz (and thus limiting the upper frequency to approximately 60 MHz), the required step size (kHz) becomes:

$$= \frac{5}{150} \qquad = 0.03333$$

For this example, the programmed step size becomes 35.76 Hz and the actual chirp rate, Equation (1), becomes 5.36 kHz/µsec.

Example 4:
If a negative chirp rate is desired, simply calculate the needed positive step size to be programmed into the Increment Register and then take the 2's complement as follows:

Suppose that a negative chirp rate of 240,000 kHz/µsec is desired as in example# 2. Calculate that the step size needed is 480 kHz and then take the 2's complement. The positive value programmed into the Increment Register would be $3EEA_H$ (calculated as the desired step size divided by the smallest step size and then converted into a HEX number). The 2's complement of this number would be $FFC116_H$.

The sine look up table (14-bit x 12 ROM) is a custom Meret part containing a patented ROM compression algorithm that reduces the normal 197k bits of information down to about 3k bits. The upper 12 bits from the dual accumulator are connected to an separate internal adder in the chirp chip which provides the ability to phase modulate or phase shift the output signal with a resolution of better than 0.09°. The upper 8 bits of the frequency accumulator are also made available that allows for monitoring of the instantaneous frequency of the chirp. With 8 bits of resolution, it is possible to determine the instantaneous output frequency to within 1.953 MHz.

Finally, the DAC is a 12/14-bit 1 GHz DAC capable of extraordinary performance. Only the 12 most significant bits are used.

9. ARCHITECTURE

A shared 24-bit parallel data buss is used to pre-load several parameters in the chirp synthesizer.

Following the 14-bit CONTROL word are the three separate 24-bit registers that store information for the MAIN Start Register, AUX Start Register and the Increment (chirp rate) Register.

Only one Start Register and Increment Register will be needed in most applications but the availability of a separate AUX Start Register adds some flexibility in the application of the chirp synthesizer to the more special requirements. It allows the user to shift between two different chirp bandwidths without having to re-program any information or as shown in the later timing diagram, it can be used to generate a CW signal while maintaining the chirp START Frequency information.

In addition to the three registers, a STROBE function (pin 17) is provided to allow synchronized data loading into the three registers. Data is loaded into the registers when the STROBE line is LOW. As this is a level triggered signal, data must be stable when the STROBE line is LOW to avoid changes in the data.

There are also two methods to force the output level to zero. The MSTR Reset can be used to reset both accumulators back to zero (but the information in the three registers are maintained) so that there is no output. The ROM Reset control disables the 14-bit x 12 ROM to disable the output but the two accumulators (and hence the chirp) continue to run.

The top 8 bits from the frequency accumulator are available on the 15-pin (P3 for the DCP-1A and STOP Out for the DCP-1) subminiature "D" connector of the chirp synthesizer. There is an 8-bit (byte wide) comparator in the DCP-1A module that will output a LOW true TTL pulse whenever the top 8 bits of the frequency accumulator (1.95 MHz resolution) are the same as the 8-bit word supplied to this connector by the customer. This signal is normally HIGH and will momentarily go LOW when the comparator is true. The user programs the desired frequency and then reads the COMPARE pin to determine when the chirp is outputting the desired instantaneous frequency. Refer to section 12.1 for pin assignments.

10. CHIRP CONTROL LOGIC

MODE Select

The MODE Select word (pins 48 & 15) is used to route the 24-bit word to the desired register. First select the desired register and place the data on the 24-bit buss. Pulse the Strobe line (pin 17) from HIGH to LOW and back to HIGH to load the data into the register. Change the Mode Select word for the next register and follow the same procedure. The following table describes the logic needed to route the data:

REGISTER	PIN 48 (MODE SELECT1)	PIN 15 (MODE SELECT0)
Control Word Register	0	0
MAIN Start Register	0	1
AUX Start Register	1	0
Increment (Chirp Rate) Register	1	1

MODE Select Logic

Control Word

The **first word** that must be sent over this data buss is the 14-bit control word needed to set up the dual phase accumulator. The following binary word should be sent with the MODE Select set to MODE Select1 = 0 and Mode Select0 = 0 (see above MODE Select Logic table):

(msb) 0000 0000 0000 0000 0100 0000 $_2$(lsb) or 000040 $_H$

MAIN/AUX Select

Once the start frequency and increment frequency have been loaded into the Start Register and Increment (Chirp Rate) Register, use the MAIN Select or AUX Select to determine which register is used in the subsequent chirp. Note that if both the MAIN and AUX Select lines are activated at the same time (within 2 nsec of each other), the MAIN Select takes precedence. These lines use positive-true logic and are active “HIGH”.

Initiating the Chirp

After the MSTR Reset line is asserted, the MAIN (or AUX) Select line controls the chirp. As soon as it is asserted (on the rising edge), the chirp begins (see timing diagram for exact delays) with a frequency at the start frequency. Every 2 nsecs the

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increment register is cumulatively added to the start register and a sweep is generated. The chirp (sweep) is constantly updated as long as both the MSTR Reset and the MAIN (or AUX) Select line are asserted (held HIGH). If both the MAIN and AUX Select line is pulled LOW, the chirp will stop and the output will be set to zero phase. Re-asserting either the MAIN or AUX Select line will begin the chirp at the start frequency.

If the CLK Reset is asserted (LOW) rather than the MAIN (or AUX) Select line, the chirp chip will freeze at the current frequency but the output will be set to zero. When the CLK Reset is released (HIGH), the chirp will continue from the last output frequency and be increment every 2 nsec with the increment register value.

Stopping the Chirp

As discussed already, there are several signals that can be used to stop the chirp. In many cases, the MAIN (or AUX) Select line will be used (refer to the timing diagram for more details on the delays). Both lines must be low to stop the chirp.

The MSTR Reset should not be used as it can produce unexpected results (automatically resets control to AUX Start Register).

An alternative method for stopping the chirp uses the STOP Frequency. This instantaneous frequency (can resolve the stop frequency with 1.953 MHz resolution) is set by the user when the 15-pin subminiature "D" connector (P3 on the DCP-1A or STOP Freq on the DCP-1) is used. The eight bits are programmed according to section 12.1, Programming the STOP Frequency, on page 18. A byte wide comparator is installed in the DCP-1A which compares this 8-bit byte with the instantaneous frequency. When the instantaneous frequency is equal to the programmed STOP Frequency, a pulse (LOW Active) will be present on the Compare bit (pin 15 on the 15-pin subminiature "D" connector).

10.1 Control Word Description (For Information only)

When both bits in the Mode Select word are set to "0", the information on the 24-bit data buss will be routed to the control register for the instrument setup.

The following is a brief description of the functions controlled by the CONTROL word discussed earlier. As can be seen, not all functions are used and several are not internally connected (i.e. Not used) within the DCP-1 and DCP-1A. Bit 0 represents the LSB of the common 24 bit data buss.

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BIT No.	Function	Function Connected?
0	Delay of DAC Clock	No
1	Delay of DAC Clock	No
2	0 = DAC Clock not inverted 1 = DAC Clock inverted	No No
3	0 = DAC Clock frequency equals Clock In freq. 1 = DAC Clock frequency equals Clock In freq. ÷ 2	No No
4	Delays the ROM Clock by number of units in conjunction with bit 5. This is the LSB of the delay number. Delay is approximately 200 ps.	
5	MSB of the ROM Clock delay value	
6	0 = ROM Clock not inverted **1 = ROM Clock inverted — desired state**	
7	0 = ROM Clock and Internal Data Clock(IDCLK) equal Clock In frequency 1 = ROM Clock and IDCLK equal Clock In freq/2	
8	0 = DATA Clock(DCLK) equals IDCLK 1 = DCLK equals External Data Clock	 No
9	0 = INTERNAL Clock (INT_CLK) equals DCLK 1 = INT_CLK equals DATA Clock Not(DCLK~)	
10	DAC Clock as programmed above. DAC Clock equals DCLK with characteristics of bits 0 thru 2.	No No
11	0 = External Phase synchronization enabled 1 = External Phase synchronization bypassed	
12	IF_CLK	No
13	IF_CLK	No

The data synchronization circuitry disables the clocking of the output register to the Full Adder until the input data from External Phase has not changed for four to eight internal cycles (INT_CLK). This synchronization is control via bit 11 above. In addition to this the signal ADDZERO resets the entire block allowing the External Phase input to be disabled.

The DAC clock from the accumulator chip is not used in this design to drive the Digital to Analog converter. The D/A clock is from other circuitry within the DCP-1A.

10.2 OTHER CONTROL LOGIC

ROM Reset

In addition to the frequency control described above, a separate TTL control line is provided to allow for very fast control of the output signal level. When this "ROM reset" line (pin #50) is activated by setting it to a "HIGH" TTL level, the output of the synthesizer will be turned off. When this line is released (TTL "LOW"), the output of the synthesizer will continue as if the chirp had never been stopped (i.e., the chirp has been internally been updating at a new frequency every 2 nsec.) If a "pause" in the chirp is desired in conjunction with the suppression of the output, the CLK Reset line should be asserted before the ROM Reset. In this matter, the releasing of the ROM Reset and then the CLK Reset will resume the chirp.

Phase Control

There is a separate 12-bit TTL data buss for control of the phase. The control signal, ADD Zero (pin 49), determines whether this additional phase information is activated. With ADD Zero asserted (LOW), the information on the phase control lines (see table) will have no effect on the output. If this line is released (held HIGH), the phase number (obtained by adding up all of the asserted control lines for the 12 bits of phase) will cause a single phase shift in the output. Note that it does not cause an **additional** phase shift for each subsequent frequency change.

Since the resolution of the synthesizer is "limited" to a non standard step size of approximately 30 Hz, some frequency values may not be available. Any frequency, however, can be set within the smallest step size (29.80… Hz).

11. TIMING INFORMATION

The following table shows the propagation delay through the dual phase accumulator (Chirp chip). In addition to these delays, 12 clocks (24 nsec) for the ROM and 1 clock (2 nsec) for the DAC must be included. Therefore, the total delay (in clocks) from a start command to the output frequency is:

8 (Accumulator) + 1 (Select/Trigger) + 12 (ROM) + 1 (DAC) + 4 nsec (Buffer Latency)

With a 500 MHz clock (2 nsec per clock), the delay becomes 48 nsec. This does not include any delay due to an anti-aliasing low pass filter.

CHIRP ACCUMULATOR TIMING PARAMETERS

Parameter	Min	Typ	Max	units
Input data set-up time	5			nsec
Input data hold time	2			nsec
MODE set up time	1			nsec

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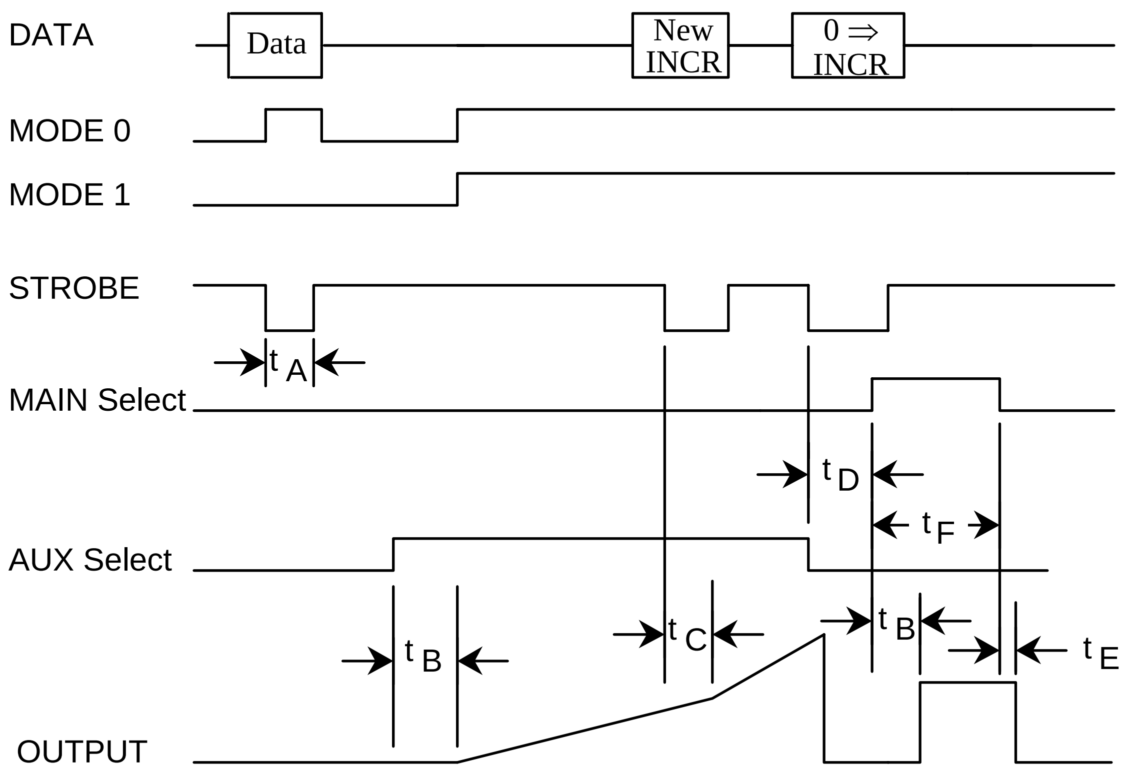
MODE hold time	1			nsec
Strobe duration time	8			nsec
Select pipe		1		clock
Freq pipe delay		8		clocks
Phase pipe delay		13		clocks
Phase pipe w/sync		17		clocks
INST_FREQ pipe	2		16	clocks
Phase control rate			125	MHz
Freq control rate			80	MHz
Clock input (max)			520	MHz

DCP-1A WAVEFORM TIMING



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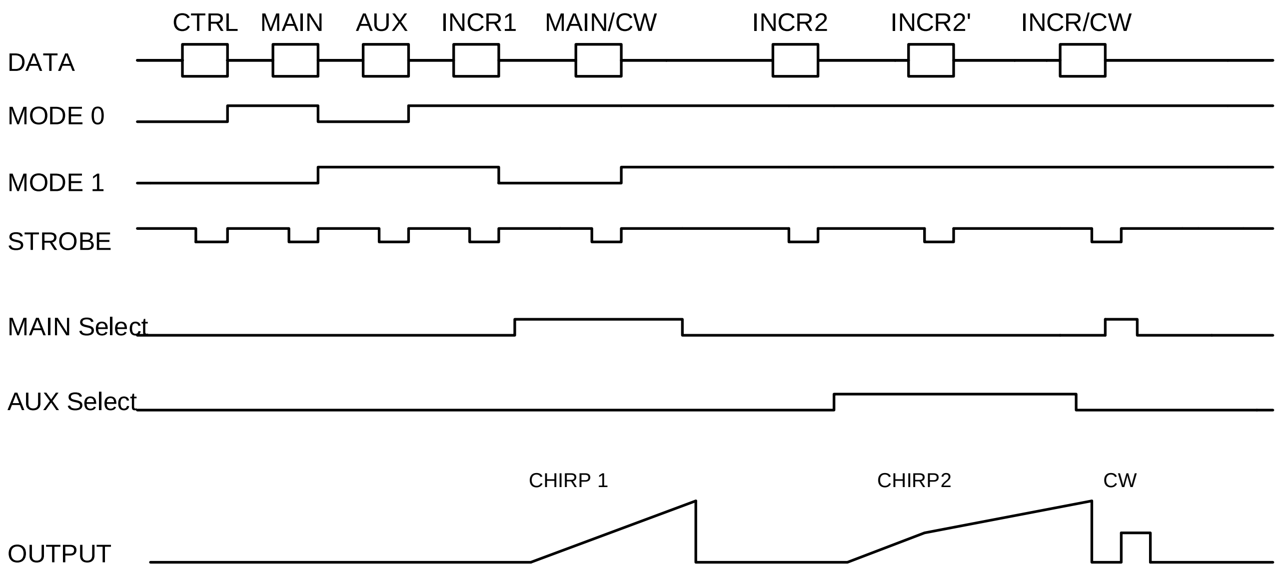
Time Period	Description	Pipe		Buffer Delay
t_A	Strobe width minimum			8 nsec
t_B	Select register to start of signal	8 clocks	+	4 nsec
t_C	Strobe low to increment change	2 clocks	+	5 nsec
t_D	Minimum low time for both selects			8 nsec
t_E	Select low to output clear			3 nsec
t_F	Minimum active select	9 clocks	+	10 nsec

Note that the above data refers to timing of the dual accumulator and does not include any delays due to the ROM (12 clock delay), DAC (1 clock delay) or low pass filter (frequency dependent).

DCP-1A WAVEFORM GENERATION



Timing for Sample Waveforms

12.1 PROGRAMMING STOP FREQUENCY

Frequency	Bit#	Pin#	Function	Pin#
250.0 MHz	CL7	2	Latch*	6
125.0 MHz	CL6	10	Enable*	9
62.5 MHz	CL5	3	GND	7 & 8
31.25 MHz	CL4	11	Vcc (+5V)**	1
15.625 MHz	CL3	4	Compare	15

7.8125 MHz	CL2	12	NC		14
3.90625 MHz	CL1	5			
1.953125 MHz	CL0	13			

* optional connection — must be specified at time of order. The Latch and Enable functions allow the user to store the STOP frequency in the DCP-1A and requires that either a 74LS574 (edge triggered) or 74LS573 (Level triggered or Transparent) Octal-D Flip Flop be installed by the factory. If not ordered, these functions are not connected.

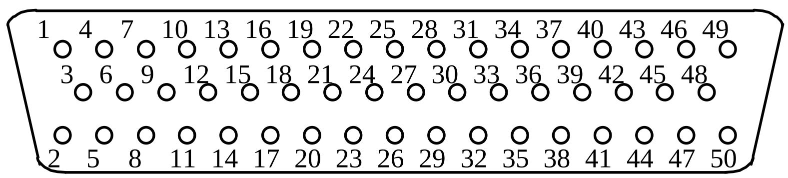
** Note that the separate interface box used to demonstrate the DCP-1 from the printer port of a PC or compatible requires V_{CC} (+5V) on pin #1. **<u>DO NOT</u> short this pin to ground or damage to the DCP-1 & DCP-1A will result.**

<u>IN ADDITION, DO NOT CONNECT PIN 1 OF THE 15-PIN CONNECTOR TO +5V.</u>

12.2 PROGRAMMING CONTROL LINES (DCP-1 Chassis)

Frequency	Bit#	Pin#	Phase	Bit#	Pin#
250.0 MHz	F23	1	180.000°	P11	28
125.0 MHz	F22	3	90.000°	P10	30
62.5 MHz	F21	2	45.000°	P09	29
31.25 MHz	F20	4	22.500°	P08	31
15.625 MHz	F19	6	11.250°	P07	33
7.8125 MHz	F18	5	5.625°	P06	32
3.90625 MHz	F17	7	2.8125°	P05	34
1.953125 MHz	F16	9	1.40625°	P04	36
976.5625 kHz	F15	8	0.70312…°	P03	35
488.28125 kHz	F14	10	0.35156…°	P02	37
244.140625 kHz	F13	12	0.17578…°	P01	39
122.0703125 kHz	F12	11	0.08789…°	P00	38
61.03515625 kHz	F11	13	ADD Zero	---	47
30.517578125 kHz	F10	15			
15.2587890625 kHz	F09	14			
7.62939453125 kHz	F08	16	MAIN Select	---	46
3.814697265… kHz	F07	18	AUX Select	---	45
1.907348632… kHz	F06	17	Mode Select1	M01	44
953.6743164… Hz	F05	19	Mode Select0	M00	43
476.8371582… Hz	F04	21			

238.4185791…	Hz	F03	20
119.2092895…	Hz	F02	22
59.60464477…	Hz	F01	24
29.80232239…	Hz	F00	23
DATA STROBE		---	49
CLK RESET		---	40
MSTR RESET		---	48
ROM RESET		---	50
GROUND		---	25,27,42,26,41

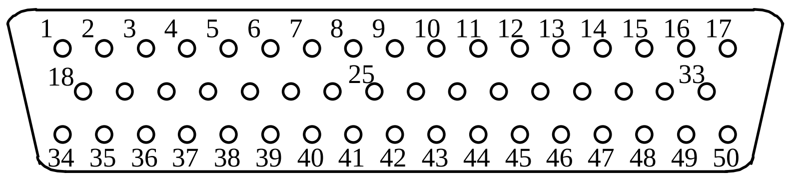


Pin Locations for DCP-1 Chassis

12.3 PROGRAMMING CONTROL LINES (DCP-1A Module)

Frequency		Bit#	Pin#	Phase	Bit#	Pin#
250.0	MHz	F23	1	180.000°	P11	10
125.0	MHz	F22	18	90.000°	P10	27
62.5	MHz	F21	34	45.000°	P09	43
31.25	MHz	F20	2	22.500°	P08	11
15.625	MHz	F19	19	11.250°	P07	28
7.8125	MHz	F18	35	5.625°	P06	44
3.90625	MHz	F17	3	2.8125°	P05	12
1.953125	MHz	F16	20	1.40625°	P04	29
976.5625	kHz	F15	36	0.70312…°	P03	45
488.28125	kHz	F14	4	0.35156…°	P02	13
244.140625	kHz	F13	21	0.17578…°	P01	30
122.0703125	kHz	F12	37	0.08789…°	P00	46
61.03515625	kHz	F11	5	ADD Zero	---	49
30.517578125	kHz	F10	22			
15.2587890625	kHz	F09	38			
7.62939453125	kHz	F08	6	MAIN Select	---	16
3.814697265…	kHz	F07	23	AUX Select	---	32

1.907348632…	kHz	F06	39	Mode Select1	M01	48
953.6743164…	Hz	F05	7	Mode Select0	M00	15
476.8371582…	Hz	F04	24			
238.4185791…	Hz	F03	40			
119.2092895…	Hz	F02	8			
59.60464477…	Hz	F01	25			
29.80232239…	Hz	F00	41			
DATA STROBE		---	17			
CLK RESET		---	14			
MSTR RESET		---	33			
ROM RESET		---	50			
GROUND		---	9,26,31,42,47			



Pin Locations for DCP-1A Module

13. SAMPLE INITIALIZATION

The following information will give you written confirmation of the timing sequence recommended for the DCP-1. This should give you an output whether it is CW or Chirp (load a zero into the Increment or chirp rate register to generate a CW signal).

1.) Load the four registers. Use the Mode Select to direct the 24-bit word to each of the 4 registers. Load them in order (i.e., Mode Select 00, 01, 10, 11). Note that the control word (should be 00 00 40$_H$) should be loaded first and the status of the MSTR Reset, CLK Reset, MAIN Select, AUX Select or ADD Zero are not critical.

The Strobe line (pin 17) should be pulsed HIGH-LOW-HIGH to load each of the four registers.

2.) Reset the unit by cycling the MSTR Reset (HIGH-LOW-HIGH).

3.) Pull the CLK Reset HIGH (MSTR Reset is already HIGH).

4.) Use the MAIN Select or AUX Select (and therefore the MAIN or AUX Start Register, respectively) to start the chirp. The chirp will initiate (or CW will be present) on the LOW-HIGH transition of this signal. For subsequent chirps, it is only necessary to cycle the Select line to start and stop the chirp. MSTR Reset should not be used as it can cause unexpected results (like switching control from the MAIN Start Register to the AUX Start Register.)

If it is desired to change the active Start Register, both Select lines must be brought LOW for a minimum of 8 nsec and then the desired Select line can be asserted. If both Select lines are asserted at the same time (within 2 nsec of each other), the MAIN Start Register will be used. If the AUX Start Register is desired and both Select lines are asserted, the AUX Select line must be asserted at least 2 nsec before asserting the MAIN Select line.

5.) The ROM Reset must be LOW and ADD Zero can be in either state depending on whether phase control is desired or not.

Note that any of the three control lines (MAIN Select, MSTR Reset, CLK Reset) can be used to stop the chirp. The MAIN (or AUX) Select line and the MSTR Reset cause the output to go to zero and start again from the Start frequency. The CLK Reset (when pulled LOW) will set the output to zero but it freezes the chirp at the last output frequency. When released, the chirp will resume at that frequency.

14. LOCK INDICATOR

Pin #5 on the 9-pin miniature D-connector of the Reference Generator (DCP-500) or a front panel LED on the DCP-1 will be a TTL "HIGH" (open collector) when the internal phase-lock is locked, and will be TTL "LOW" when the internal phase-lock is unlocked (LED illuminated). No lock indicator is available on the DCP-500A.

15. WARRANTY

All Meret products are warranted against defects in material and workmanship for a period of one year after initial shipment. Meret will repair or replace any circuit or component that is found to be defective during this period if in Meret's sole opinion the product is deemed defective.

Any modifications or options performed by Meret during the initial one year period shall be included under the initial warranty, and such secondary warranties shall terminate one year after the initial shipment. Shipment of the product to Meret (San Diego, CA) shall be made prepaid and shall not be made without prior authorization by Meret.

This warranty is voided if the product is abused or if unauthorized modifications are made by the user.

This warranty is in lieu of all other warranties, expressed or implied, and no person is authorized to represent or assume for Meret any liability in connection with the sales of our products other than stated within this warranty.

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Serial Number

Options: ____

Remarks: ____

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QC by ______________________________ Date: ____________